



# L-IG41M3

Rev:1.1

## TABLE OF CONTENTS

PAGE 01	COVER PAGE
PAGE 02	GPIO/STRAP
PAGE 03	System Block Diagram
PAGE 04	CPU-SOCKET LG775-1
PAGE 05	CPU-SOCKET LG775-2
PAGE 06	CPU-SOCKET LG775-3
PAGE 07	CLOCK SLG8XP548T
PAGE 08	MCH PCIE/DMI/FSB
PAGE 09	MCH /DDR3A/DDR3B
PAGE 10	MCH /VGA/MISC
PAGE 11	MCH /POWER
PAGE 12	MCH /GND
PAGE 13	PCIE 16X
PAGE 14	HDMI Interface
PAGE 15	VGA CONN/HDMI CONN
PAGE 16	240P DDR3, CHA
PAGE 17	240P DDR3, CHB
PAGE 18	ICH7 PCI/PCI-E/USB
PAGE 19	ICH7 SATA
PAGE 20	ICH7 DEVICE
PAGE 21	ICH7 POWER
PAGE 22	USB
PAGE 23	SPI ROM/PCI-E 1X * 2
PAGE 24	PCI
PAGE 25	REALTEK LAN 8102EL/8103EL/8111DL
PAGE 26	SUPER I/O 8755/8757
PAGE 27	PS2/COM
PAGE 28	PANEL & FAN
PAGE 29	Audio CODEC(ALC662)
PAGE 30	Audio Connector
PAGE 31	DC_Vcore(NCP5395T)
PAGE 32	DC to DC
PAGE 33	DC to DC II
PAGE 34	DUAL POWER
PAGE 35	TEST POINT & OTHER
PAGE 36	Power Delivery
PAGE 37	RESET Power Sequence Diagram
PAGE 38	CLOCK DISTRIBUTION

### Revision History

Rev	Data	Description
A	2009/03/14	
0.1	2009/05/08	Page04:add cpu heat sink fix HOLE via for lenovo request (edit cpu lib (add HOLE_GND pin 1~16) ) Page15:VGA R/G/B signal rise/fall time fail solution and VGA leakage current issue solution Page22:F_USB1/F_USB2 change to 6*2 header for lenovo usb header spec change Page27:add serial resistors for PS/2 KB/MS (lenovo request) Page31:VRD11.1 signal measure solution Page07/Page20:RTC signal measure fail solution Page09/21:follow intel review result Page32/Page33:Reserve damping resistor at gate pin of MOSFET and negative feedback signal of OP
1.0	2009/07/01	page07:change PB12 footprint to 0603 for somkeless issue page25:update LAN Dual Color LED Schematic page26:IT8757 Update ATXPG circuit for 3V level page31:change R113/R112/R116=1R0 ,C98/C102/C106=4700pF for Low side MOS VDS over spec
	2009/07/28	page25:add bom table for lan EFUSE & EEPROM
1.1	2009/08/17	page25:update lan active LED control circuit

Design guide:

649795\_Intel\_G31\_Platform\_Design\_Guide\_Rev1\_0 for ICH7

367652\_Intel\_4\_Series\_Platform\_Design\_Guide\_Rev2\_3

		<b>Elitegroup Computer Systems</b>	
Title		<b>COVER PAGE</b>	
Size	Document Number	Rev	
Custom	<b>L-IG41M3</b>	<b>1.1</b>	
Date:	Monday, August 31, 2009	Sheet	1 of 38

ICH7 GPIO Table

Name	Type	Voltage	Default	Functional	Function
GPI06	I/O	+VCC3	GPI	GPI6	CLR_COMS
GPI010	I/O	+3VSB	GPI	GPI10	LAN DSM function Detect
GPI023	I/O	+VCC3	LDRQ1#	LDRQ1#	FRONT_AUD_DET
GPI024	I/O	+3VSB	GPO	GPO24	CPU Variable SET
GPI028	I/O	+3VSB	GPO	GPO28	
GPI026	I/O	+3VSB	GPO	GPO26	USBPWR_FR
GPI027	I/O	+3VSB	GPO	GPO27	USBPWR_RE
GPI034	I/O	+VCC3	GPO	GPO34	LAN DSM function control
GPI035	I/O	+VCC3	GPI	GPO35	Chassis ID 1 Chassis ID 2
GPI039	I/O	+VCC3	GPI	GPO39	
GPI038	I/O	+VCC3	GPI	GPO38	COM1 detect
GPI08	I/O	+3VSB	GPI	GPI8	COM header detect 0 with com header *1 without com header
GPI09	I/O	+3VSB	GPI	GPI9	SPDIFOUT header detect 0 with spdifout header *1 without spdifout header

ITE8755 GPIO Table

Name	Type	Voltage	Default	Functional Description	Function
GP25	DIOD8	VCCH	GPO25	GPI025	Y LED CONTROL
GP26	DIOD8	VCCH	GPO26	GPI026	G LED CONTROL
GP12	DIOD8	+VCC	PCI Reset 1#	PCI Reset 1# / GPIO 12	WT_BEEP
GP14	DIOD8	+VCC	PECI Request	PECI Request /GPIO14	ICH_THRM_L
GP40	DIOD8	VCCH	3VSBSW#	3VSBSW# / GPIO 40	DIMM_SVDUAL CONTROL

G41 Strapping table

Name	Strapping
SDVO_CTRLDATA sample during reset	1 Enable the digital Port B 0 Disabled the digital Port B(DEFAULT INTERNAL PD)
DDPC_CTRLDATA sample during reset	1 Enable the digital Port C 0 Disabled the digital Port C(DEFAULT INTERNAL PD)
TCEN	TLS Confidentiality Enable(Transport Layer Security Straps) *0 = Disable TLS (DEFAULT) 1 = Enable TLS
ITPM	Integrated TPM Enable 0 = Enable Intel TPM *1 = Disable Intel TPM (DEFAULT)
EXP_SLR	PCI Express* Static Lane Reversal/Form Factor Selection *1 Normal operation (ATX) (DEFAULT) 0 (G)MCH PCI Express lane numbers are reversed (BTX)
EXP_SM	Concurrent PCI Express Port Enable *1 Both SDVO and PCI Express are operating simultaneously via the PCI Express port (DEFAULT) 0 Only SDVO or PCI Express is operational
TP_MF20 (DualX8_Enable)	2x8 PEG Port Bifurcation: *1 1x16 PCI Express Port Enabled(DEFAULT) 0 2x8 PCI Express Ports Enabled

ICH7 Strapping table

Name	Strapping
GPO25 internal pull-up	DMI AC/DC Coupling Selection(Sampled on Rising Edge of RSMRST#) 1 the DMI interface is strapped to operate in DC coupled mode 0 the DMI interface is strapped to operate in AC coupled mode(Default)
GNT5_L : GNT4_L internal pull-up	BOOT BIOS DESTINATION SELECTION(Sampled on rising edge of PWROK) *0:1 Flash Cycles Routed to SPI(Default) 1:0 Flash Cycles Routed to PCI 1:1 Flash Cycles Routed to LPC 0:0 Reserved
TP_SF21 (ICH PIN F21,TP3) internal pull-up	XOR Chain Entrance(Sampled on rising edge of PWROK): low enable (This signal should not be pulled low unless using XOR Chain testing.)
ICH_HDSDOUT :bit1 ICH_HDSYNC :bit0 internal pull-down	PCI Express Port Configuration (Sampled on rising edge of PWROK when TP3 is not pulled low at the rising edge of PWROK) 11 = 1 x4, Port 1 (x4) 10 = Reserved 01 = Reserved *00 = 4 x1s, Port 1 (x1), Port 2 (x1), Port 3 (x1), Port 4 (x1)
ICH_INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable *1 Enable 0 Disabled
SPKR internal pull-down	No Reboot mode(ICH7 will disable the TCO Timer system reboot feature) 1 Enable *0 Disabled

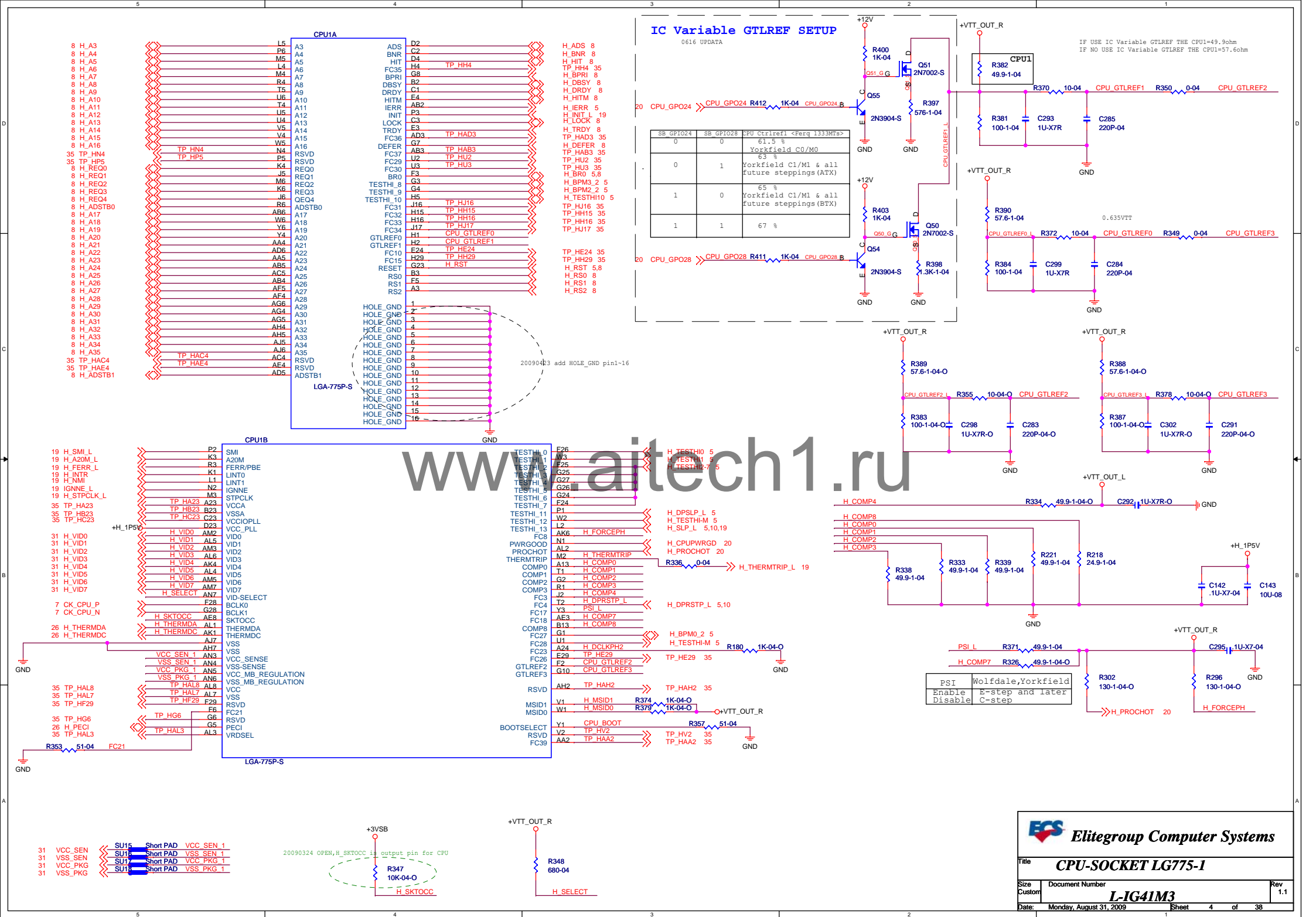
Support HDMI audio table

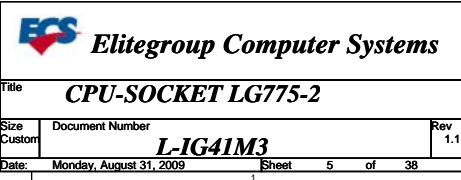
*		
	HDMI Disable	HDMI Enable
HDMIa(Page10)	X	V
HDMIb(Page10)	V	X
HDMIc(Page11)	X	V
HDMId(Page11)	V	X
HDMIe(Page20)	X	V
HDMIf(Page21)	+3VSB	+1P5_SB
HDMIg(Page21)	+VCC3	+ICH_1P5V
HDMIh(Page29)	+VCC3	+ICH_1P5V
HDMIi(Page33)	X	V

PCI ROUTING TABLE

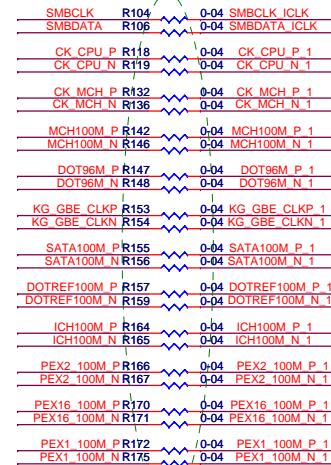
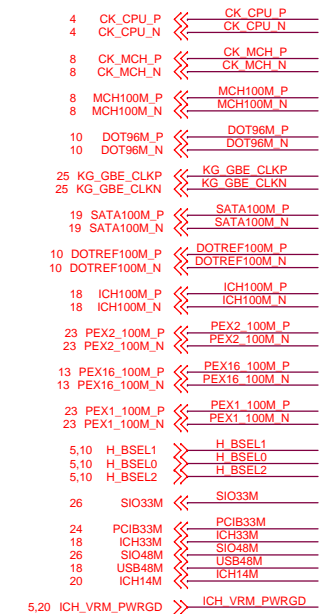
DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	18	F/G/H/E	REQ0	GNT0







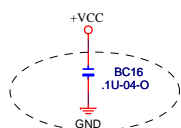
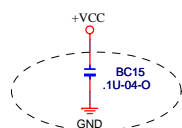
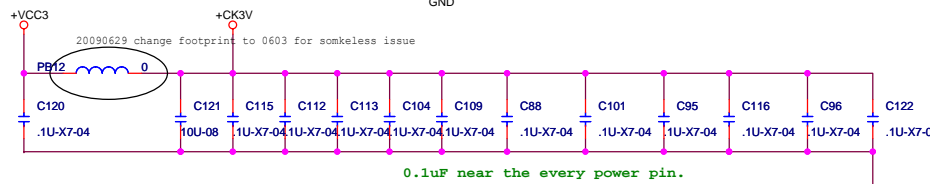
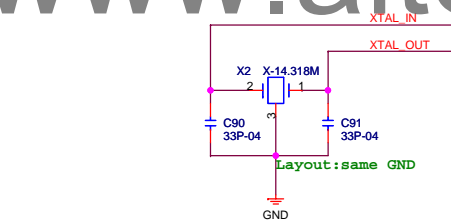
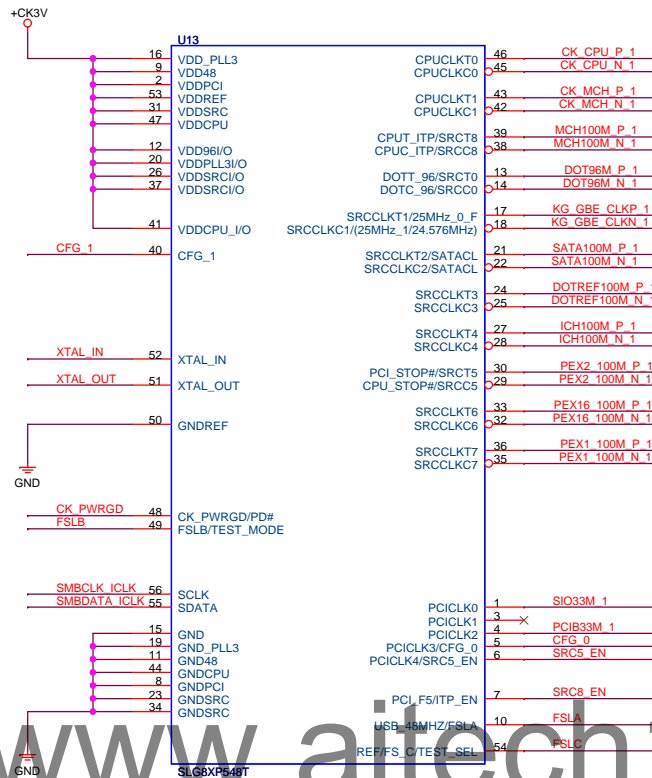




20090324 add for lenovo(SI reserve)

CFG\_0 & CFG\_1 Configuration

CFG_1	CFG_0	Pin 17	Pin 18	Pin 21	Pin 22
Low	Low	25MHz_0_F	25MHz_1	SRC_2	SRC_2#
Mid	Low	SRC_1	SRC_1#	SRC_2	SRC_2#
High	Low	25MHz_0_F	24.576MHz	SRC_2	SRC_2#
Low	High	25MHz_0_F	25MHz_1	SATA	SATA#
Mid	High	SRC_1	SRC_1#	SATA	SATA#
High	High	25MHz_0_F	24.576MHz	SATA	SATA#



Voltage Threshold for CFG\_1 (tri-level input)

State	Min	Typical	Max
Low	0V	0.55V	0.9V
Mid	1.3V	1.65V	2.0V
High	2.4V	2.75V	VDD

## CPU

## MCH (FSB)

## MCH (PCIE)

## MCH (VGA)

## LAN

## ICH (SATA)

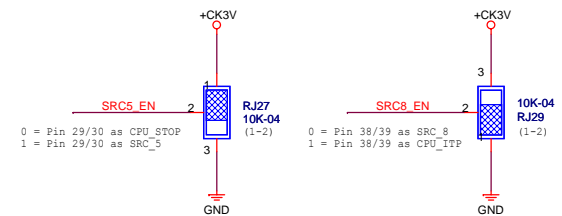
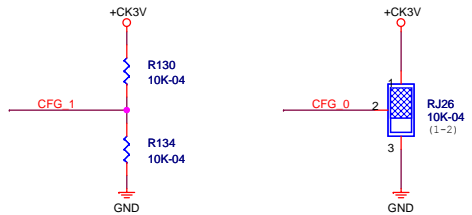
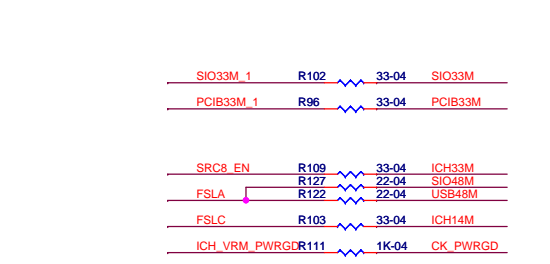
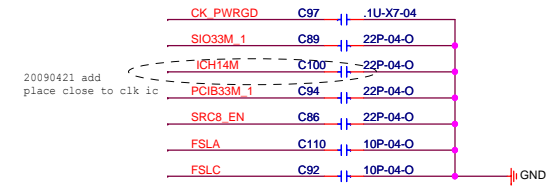
## MCH (DIGITAL VIDEO)

## ICH

## X1

## X16

## X1



0 = Pin 29/30 as CPU\_STOP  
1 = Pin 29/30 as SRC\_5

0 = Pin 38/39 as SRC\_8  
1 = Pin 38/39 as CPU\_ITP

Bit2	Bit1	Bit0	CPU CLOCK (MHz)	CPU FSB CLOCK
0	0	0	266.66	FSB 1066
0	0	1	133.33	FSB 800
0	1	0	200.00	FSB 800
0	1	1	166.66	FSB 1333
1	0	0	333.33	FSB 1333
1	0	1	100.00	FSB 1333
1	1	0	400.00	FSB 1333

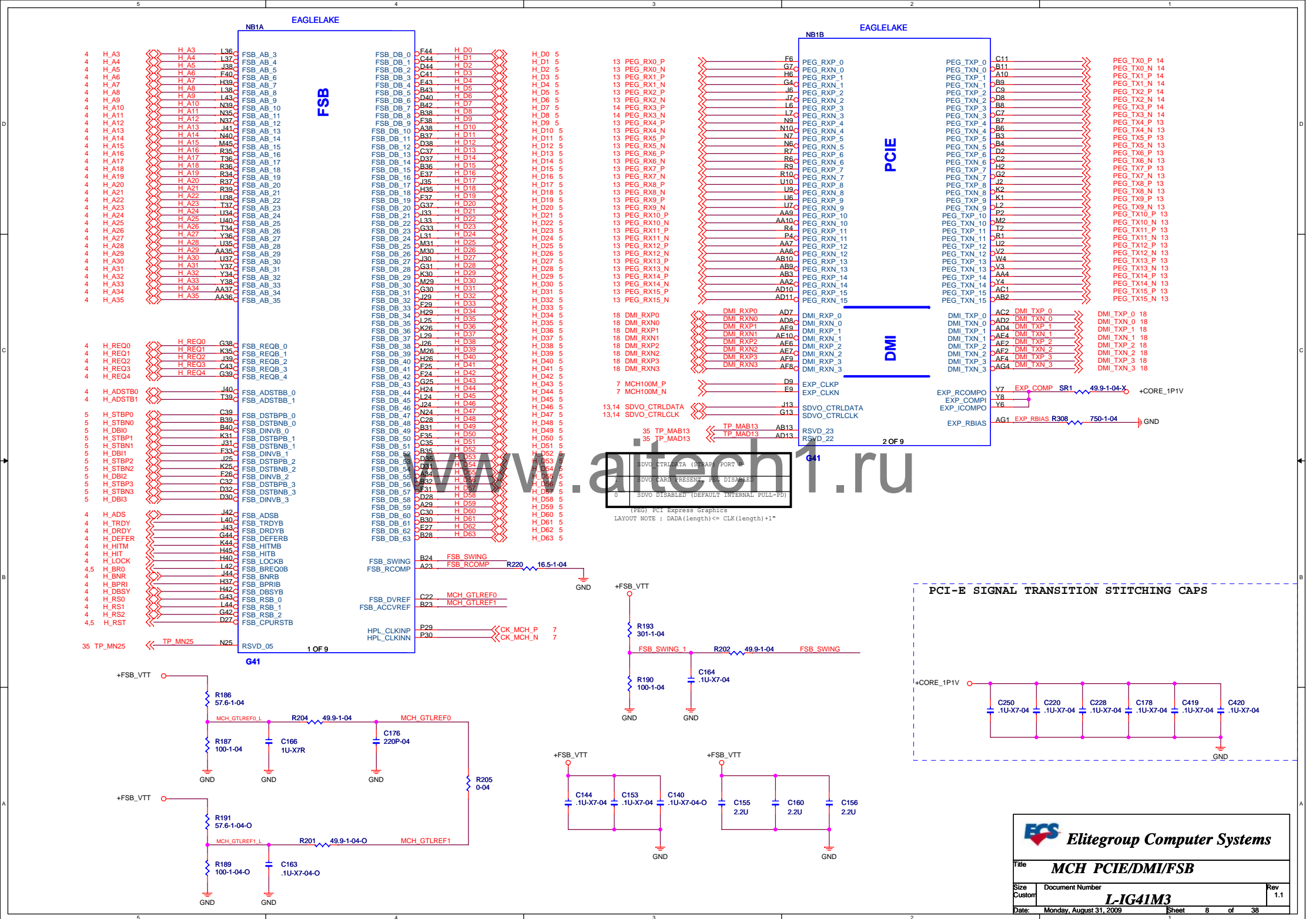
**Elitegroup Computer Systems**

Title: **SLG8XP548T(CK505)**

Size Custom: Document Number **L-IG41M3** Rev 1.1

Date: Monday, August 31, 2009 Sheet 7 of 38







20,26,32,34 SLP4\_L M3\_DRSTB  
16,17 M3\_DRSTB

16 M3A\_DQS0\_P M3A\_DQS0\_P  
16 M3A\_DQS0\_N M3A\_DQS0\_N  
16 M3A\_DQS1\_P M3A\_DQS1\_P  
16 M3A\_DQS1\_N M3A\_DQS1\_N  
16 M3A\_DQS2\_P M3A\_DQS2\_P  
16 M3A\_DQS2\_N M3A\_DQS2\_N  
16 M3A\_DQS3\_P M3A\_DQS3\_P  
16 M3A\_DQS3\_N M3A\_DQS3\_N  
16 M3A\_DQS4\_P M3A\_DQS4\_P  
16 M3A\_DQS4\_N M3A\_DQS4\_N  
16 M3A\_DQS5\_P M3A\_DQS5\_P  
16 M3A\_DQS5\_N M3A\_DQS5\_N  
16 M3A\_DQS6\_P M3A\_DQS6\_P  
16 M3A\_DQS6\_N M3A\_DQS6\_N  
16 M3A\_DQS7\_P M3A\_DQS7\_P  
16 M3A\_DQS7\_N M3A\_DQS7\_N

16 M3A\_CASB M3A\_CASB  
16 M3A\_RASB M3A\_RASB  
16 M3A\_WEB M3A\_WEB

16 M3A\_CK0\_P M3A\_CK0\_P  
16 M3A\_CK0\_N M3A\_CK0\_N  
16 M3A\_CK2\_P M3A\_CK2\_P  
16 M3A\_CK2\_N M3A\_CK2\_N

16 M3A\_MA[14..0] M3A\_MA[14..0]

16 M3A\_BS[2..0] M3A\_BS[2..0]

16 M3A\_CS[1..0] M3A\_CS[1..0]

16 M3A\_CKE[1..0] M3A\_CKE[1..0]

16 M3A\_DM[7..0] M3A\_DM[7..0]

16 M3A\_ODT[6..0] M3A\_ODT[6..0]

16 M3A\_ODT[1..0] M3A\_ODT[1..0]

17 M3B\_DQS0\_P M3B\_DQS0\_P  
17 M3B\_DQS0\_N M3B\_DQS0\_N  
17 M3B\_DQS1\_P M3B\_DQS1\_P  
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17 M3B\_DQS2\_N M3B\_DQS2\_N  
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17 M3B\_DQS6\_N M3B\_DQS6\_N  
17 M3B\_DQS7\_P M3B\_DQS7\_P  
17 M3B\_DQS7\_N M3B\_DQS7\_N

17 M3B\_WEB M3B\_WEB  
17 M3B\_CASB M3B\_CASB  
17 M3B\_RASB M3B\_RASB

17 M3B\_CK0\_P M3B\_CK0\_P  
17 M3B\_CK0\_N M3B\_CK0\_N  
17 M3B\_CK2\_P M3B\_CK2\_P  
17 M3B\_CK2\_N M3B\_CK2\_N

17 M3B\_DM[7..0] M3B\_DM[7..0]

17 M3B\_D[6..0] M3B\_D[6..0]

17 M3B\_MA[14..0] M3B\_MA[14..0]

17 M3B\_BS[2..0] M3B\_BS[2..0]

17 M3B\_CS[1..0] M3B\_CS[1..0]

17 M3B\_CKE[1..0] M3B\_CKE[1..0]

17 M3B\_ODT[1..0] M3B\_ODT[1..0]

35 TP\_M3A\_CK3\_P TP\_M3A\_CK3\_P  
35 TP\_M3A\_CK3\_N TP\_M3A\_CK3\_N  
35 TP\_M3A\_CK5\_P TP\_M3A\_CK5\_P  
35 TP\_M3A\_CK5\_N TP\_M3A\_CK5\_N

35 TP\_M3A\_CSB2 TP\_M3A\_CSB2  
35 TP\_M3A\_CSB3 TP\_M3A\_CSB3  
35 TP\_M3A\_ODT2 TP\_M3A\_ODT2  
35 TP\_M3A\_ODT3 TP\_M3A\_ODT3

35 TP\_M3A\_CKE2 TP\_M3A\_CKE2  
35 TP\_M3A\_CKE3 TP\_M3A\_CKE3  
35 TP\_M3B\_CK3\_P TP\_M3B\_CK3\_P  
35 TP\_M3B\_CK3\_N TP\_M3B\_CK3\_N

35 TP\_M3B\_CK4\_P TP\_M3B\_CK4\_P  
35 TP\_M3B\_CK4\_N TP\_M3B\_CK4\_N  
35 TP\_M3B\_CSB2 TP\_M3B\_CSB2  
35 TP\_M3B\_CSB3 TP\_M3B\_CSB3

35 TP\_M3B\_CSB4 TP\_M3B\_CSB4  
35 TP\_M3B\_CKE2 TP\_M3B\_CKE2  
35 TP\_M3B\_CKE3 TP\_M3B\_CKE3  
35 TP\_M3B\_ODT2 TP\_M3B\_ODT2  
35 TP\_M3B\_ODT3 TP\_M3B\_ODT3

EAGLELAKE

NB1C

M3A\_DQS0\_P BC5  
M3A\_DQS0\_N BD4C  
M3A\_DM0 BC3C  
M3A\_D0 BC2  
M3A\_D1 BD3  
M3A\_D2 BD3  
M3A\_D3 BD7  
M3A\_D4 BD2  
M3A\_D5 BA3  
M3A\_D6 BE6  
M3A\_D7 BD6  
M3A\_DQS1\_P BB9  
M3A\_DQS1\_N BC9C  
M3A\_DM1 BD9C  
M3A\_D8 BB8  
M3A\_D9 AY8  
M3A\_D10 BD11  
M3A\_D11 BB11  
M3A\_D12 BC7  
M3A\_D13 BE8  
M3A\_D14 BD10  
M3A\_D15 AY11  
M3A\_DQS2\_P BD15  
M3A\_DQS2\_N BB15C  
M3A\_DM2 BD14  
M3A\_D16 BB14  
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M3A\_D26 AY24  
M3A\_D27 AY24  
M3A\_D28 AY24  
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M3A\_D33 AK43  
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M3A\_D44 AF40  
M3A\_D45 AF44  
M3A\_D46 AD44  
M3A\_D47 AC41  
M3A\_DQS6\_P Y43  
M3A\_DQS6\_N Y42C  
M3A\_DM6 AA45  
M3A\_D48 AB43  
M3A\_D49 AA42  
M3A\_D50 W42  
M3A\_D51 W41  
M3A\_D52 AB42  
M3A\_D53 AB44  
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M3A\_D55 Y40  
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M3A\_DQS7\_N T43C  
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M3A\_D60 V44  
M3A\_D61 V43  
M3A\_D62 R41  
M3A\_D63 R44

DDR\_A\_MA\_0  
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DDR\_A\_MA\_4  
DDR\_A\_MA\_5  
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BC41  
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BA31 M3A\_MA7  
BD30 M3A\_MA8  
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M3B\_D2 BA9  
M3B\_D3 AU11  
M3B\_D4 AU7  
M3B\_D5 AU8  
M3B\_D6 AW7  
M3B\_D7 AY9  
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M3B\_DQS1\_N AU15  
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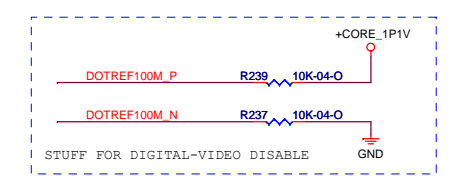
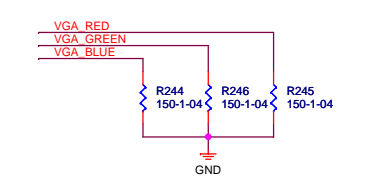
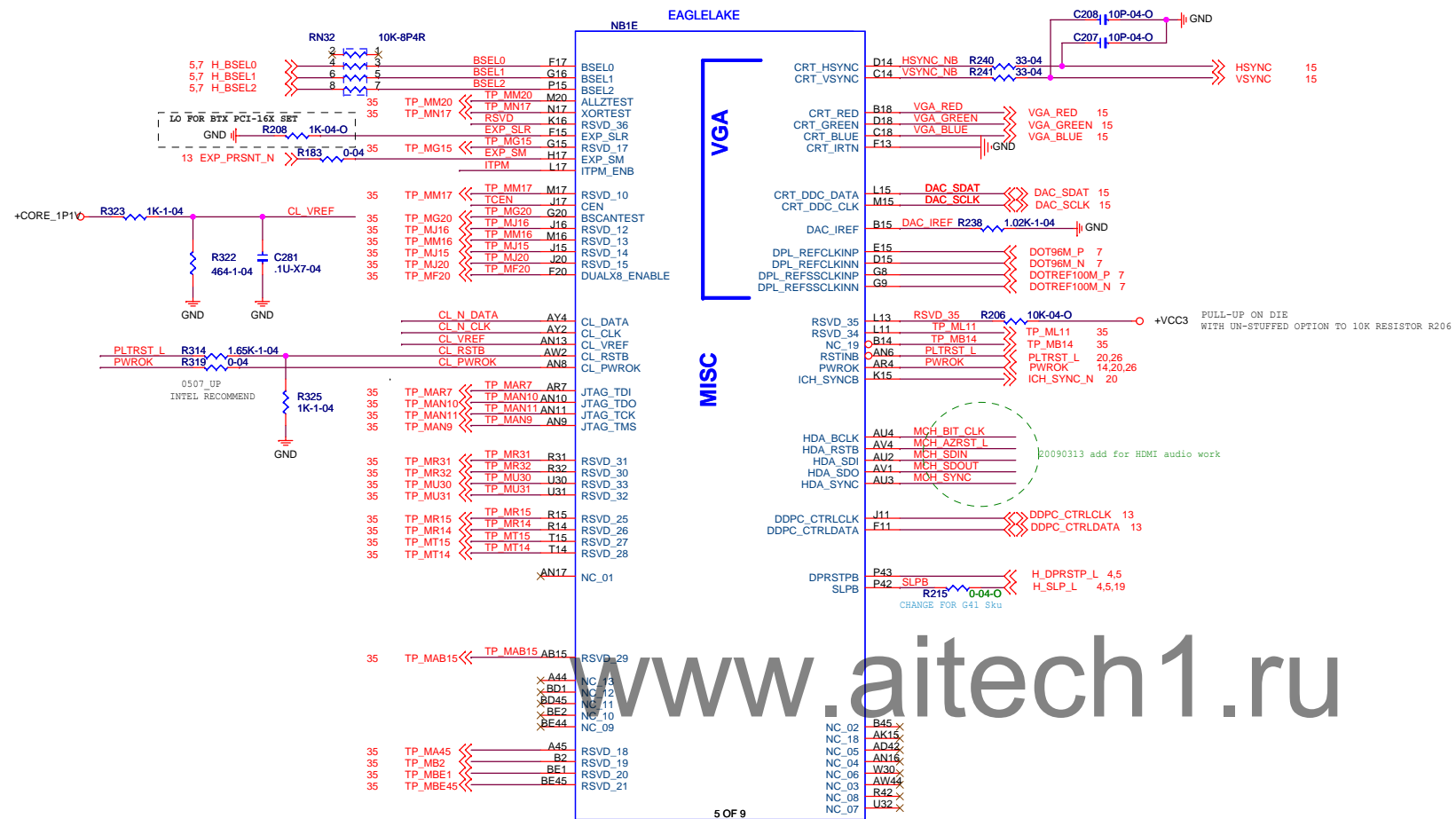
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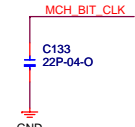
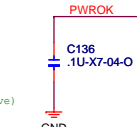
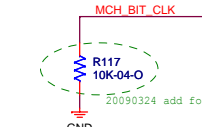
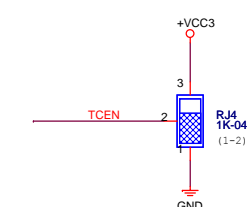
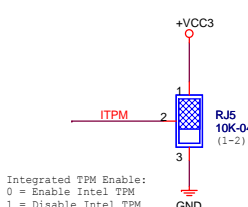
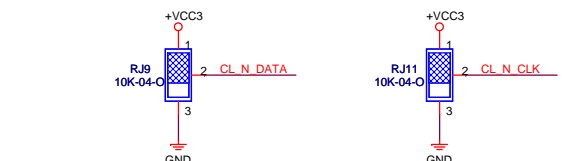
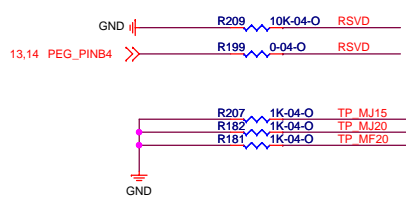
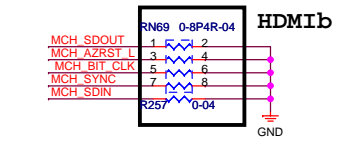
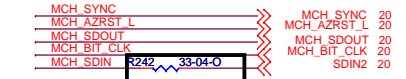
DDR\_B\_DQS\_1  
DDR\_B\_DQS\_1  
DDR\_B\_DM\_1  
DDR\_B\_DQ\_8  
DDR\_B\_DQ\_9  
DDR\_B\_DQ\_10  
DDR\_B\_DQ\_11  
DDR\_B\_DQ\_12  
DDR\_B\_DQ\_13  
DDR\_B\_DQ\_14  
DDR\_B\_DQ\_15  
DDR\_B\_DQS\_2  
DDR\_B\_DQS\_2  
DDR\_B\_DM\_2  
DDR\_B\_DQ\_16  
DDR\_B\_DQ\_17  
DDR\_B\_DQ\_18  
DDR\_B\_DQ\_19  
DDR\_B\_DQ\_20  
DDR\_B\_DQ\_21  
DDR\_B\_DQ\_22  
DDR\_B\_DQ\_23  
DDR\_B\_DQS\_3  
DDR\_B\_DQS\_3  
DDR\_B\_DM\_3  
DDR\_B\_DQ\_24  
DDR\_B\_DQ\_25  
DDR\_B\_DQ\_26  
DDR\_B\_DQ\_27  
DDR\_B\_DQ\_28  
DDR\_B\_DQ\_29  
DDR\_B\_DQ\_30  
DDR\_B\_DQ\_31  
DDR\_B\_DQS\_4  
DDR\_B\_DQS\_4  
DDR\_B\_DM\_4  
DDR\_B\_DQ\_32  
DDR\_B\_DQ\_33  
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DDR\_B\_DM\_5  
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DDR\_B\_DQS\_6  
DDR\_B\_DM\_6  
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DDR\_B\_DQ\_61  
DDR\_B\_DQ\_62  
DDR\_B\_DQ\_63

DDR\_B\_CSB\_0  
DDR\_B\_CSB\_1  
DDR\_B\_CSB\_2  
DDR\_B\_CSB\_3  
DDR\_B\_CKE\_0  
DDR\_B\_CKE\_1  
DDR\_B\_CKE\_2  
DDR\_B\_CKE\_3  
DDR\_B\_ODT\_0  
DDR\_B\_ODT\_1  
DDR\_B\_ODT\_2  
DDR\_B\_ODT\_3  
DDR\_B\_CK\_0  
DDR\_B\_CK\_1  
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DDR\_B\_CK\_51  
DDR\_B\_CK\_52



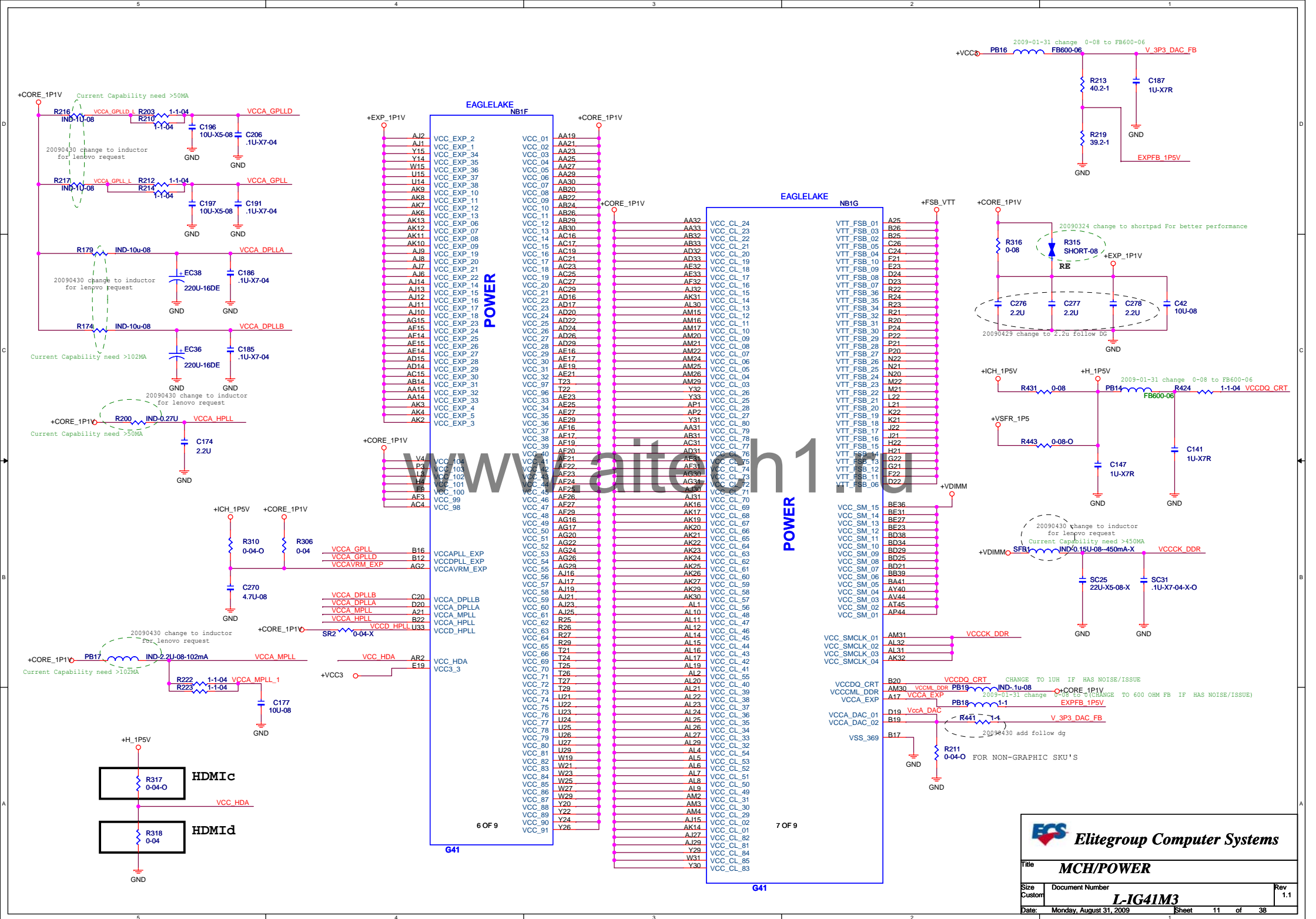
DDPC_CTRLDATA (STRAP) PORT C	
1	SDVO CARD PRESENT, PEG DISABLED
0	SDVO DISABLED (DEFAULT INTERNAL PULL-UP)

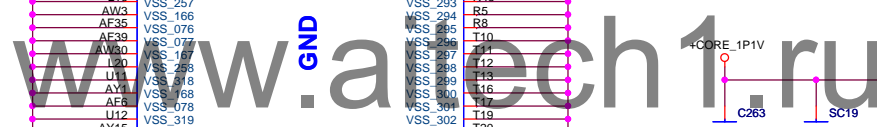
(PEG) PCI Express Graphics  
LAYOUT NOTE : DATA(length) <= CLK(length)+1\*

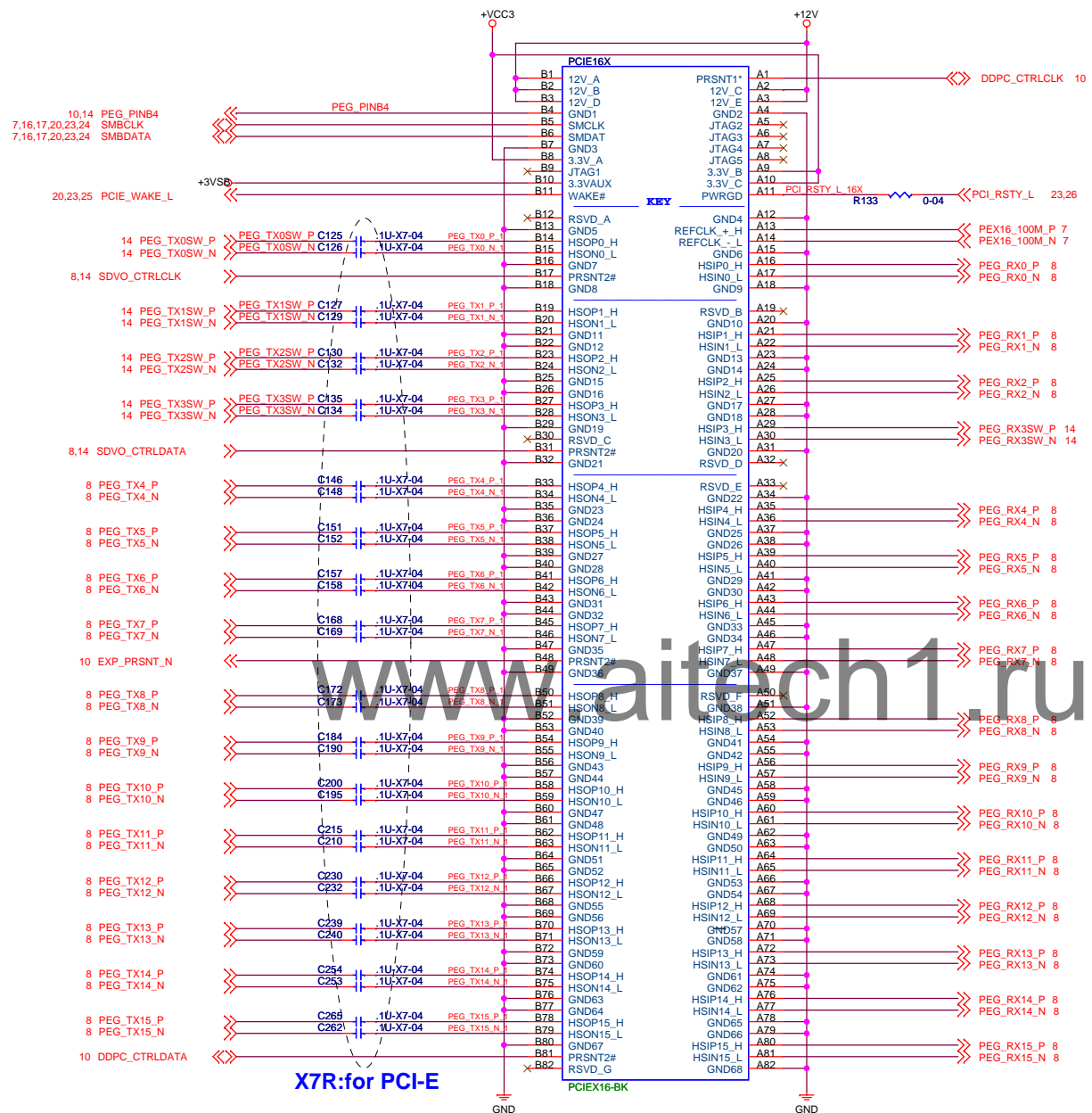


Integrated TPM Enable:  
0 = Enable Intel TPM  
1 = Disable Intel TPM  
NOTE: This signal is not used on the 82G45, 82G43, 82G41 GMCH and 82P45, 82P43 MCH.

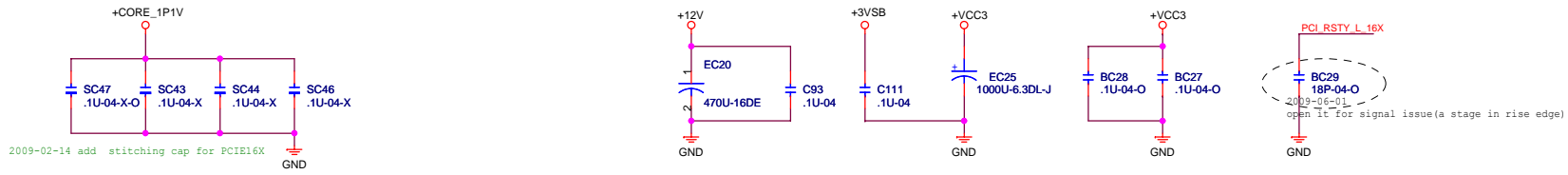
TLS Confidentiality Enable(Transport Layer Security Straps):  
0 = Disable TLS  
1 = Enable TLS








X7R:for PCI-E

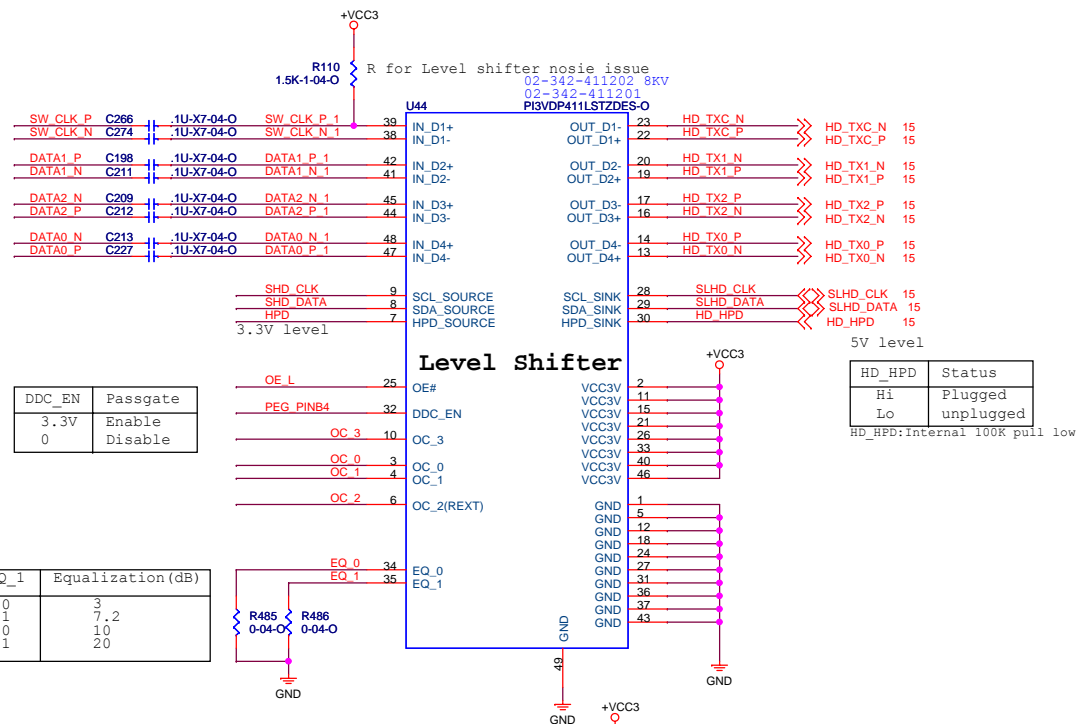
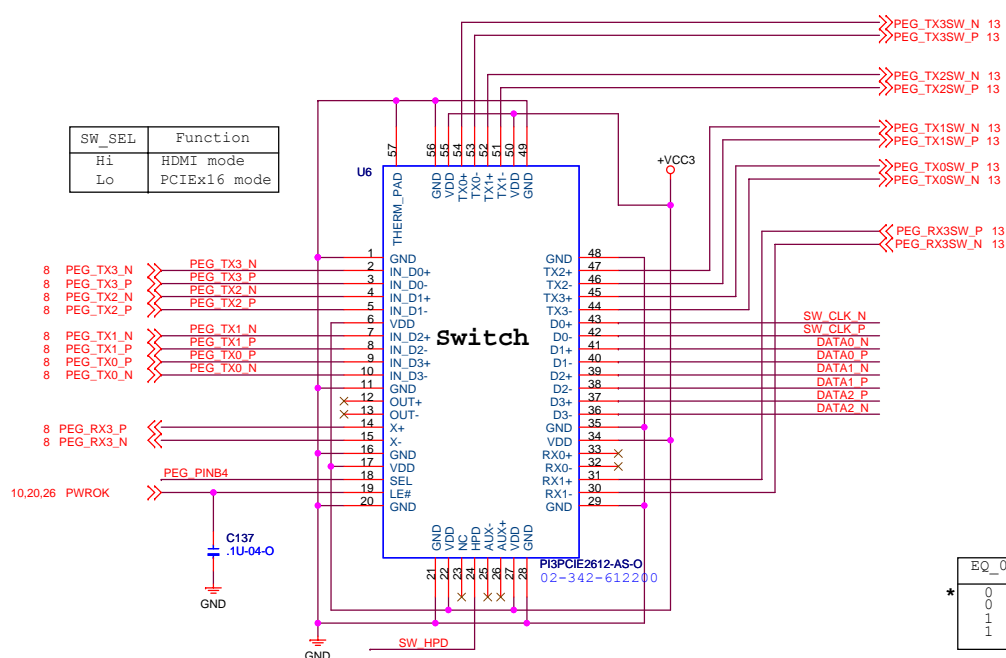



**Elitegroup Computer Systems**

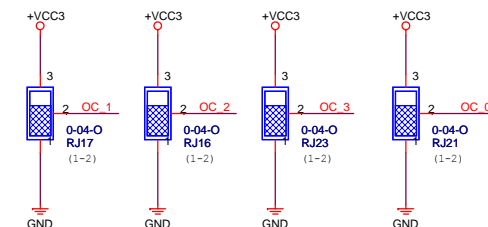
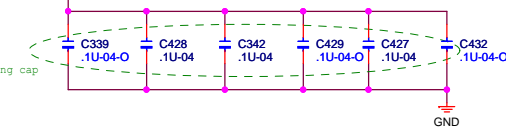
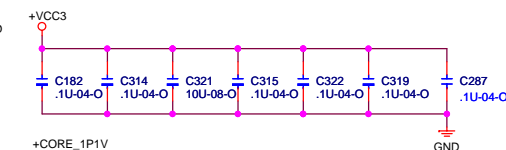
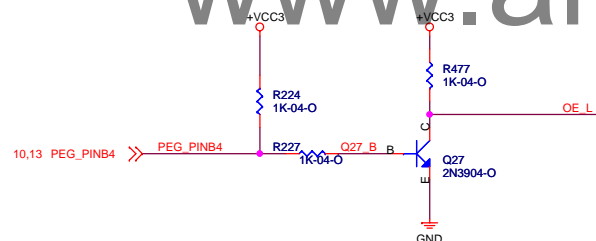
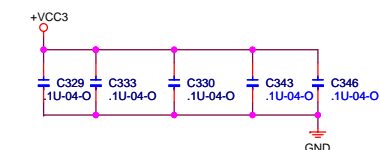
<b>Title</b> <span style="font-size: 1.2em;">PCIE 16X</span>		
<b>Size</b> Custom	<b>Document Number</b> <span style="font-size: 1.2em;">L-IG41M3</span>	<b>Rev</b> 1.1
<b>Date:</b> Monday, August 31, 2009 <span style="float: right;">Sheet 13 of 38</span>		



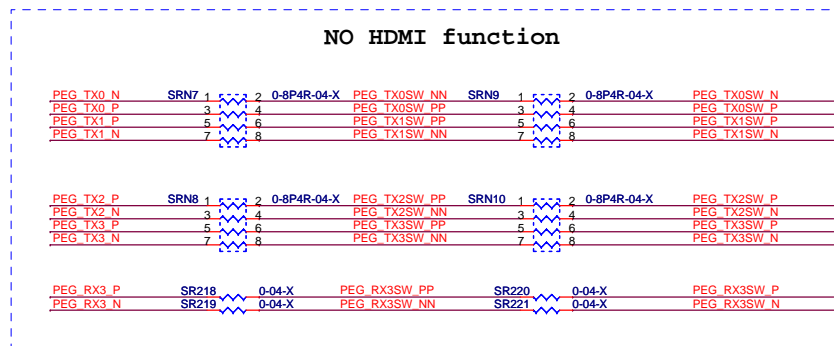
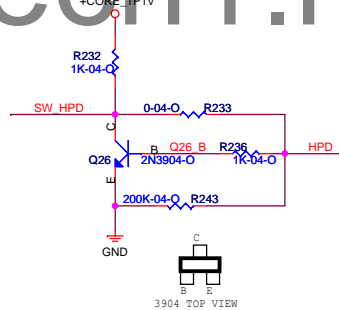
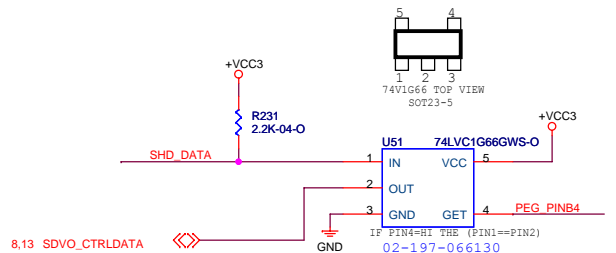
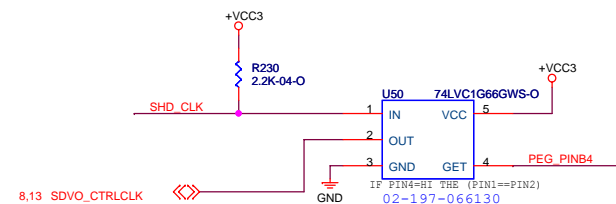
SW_SEL	Function
Hi	HDMI mode
Lo	PCIEx16 mode



	EQ_0	EQ_1	Equalization(dB)
*	0	0	3
	0	1	7.2
	1	0	10
	1	1	20

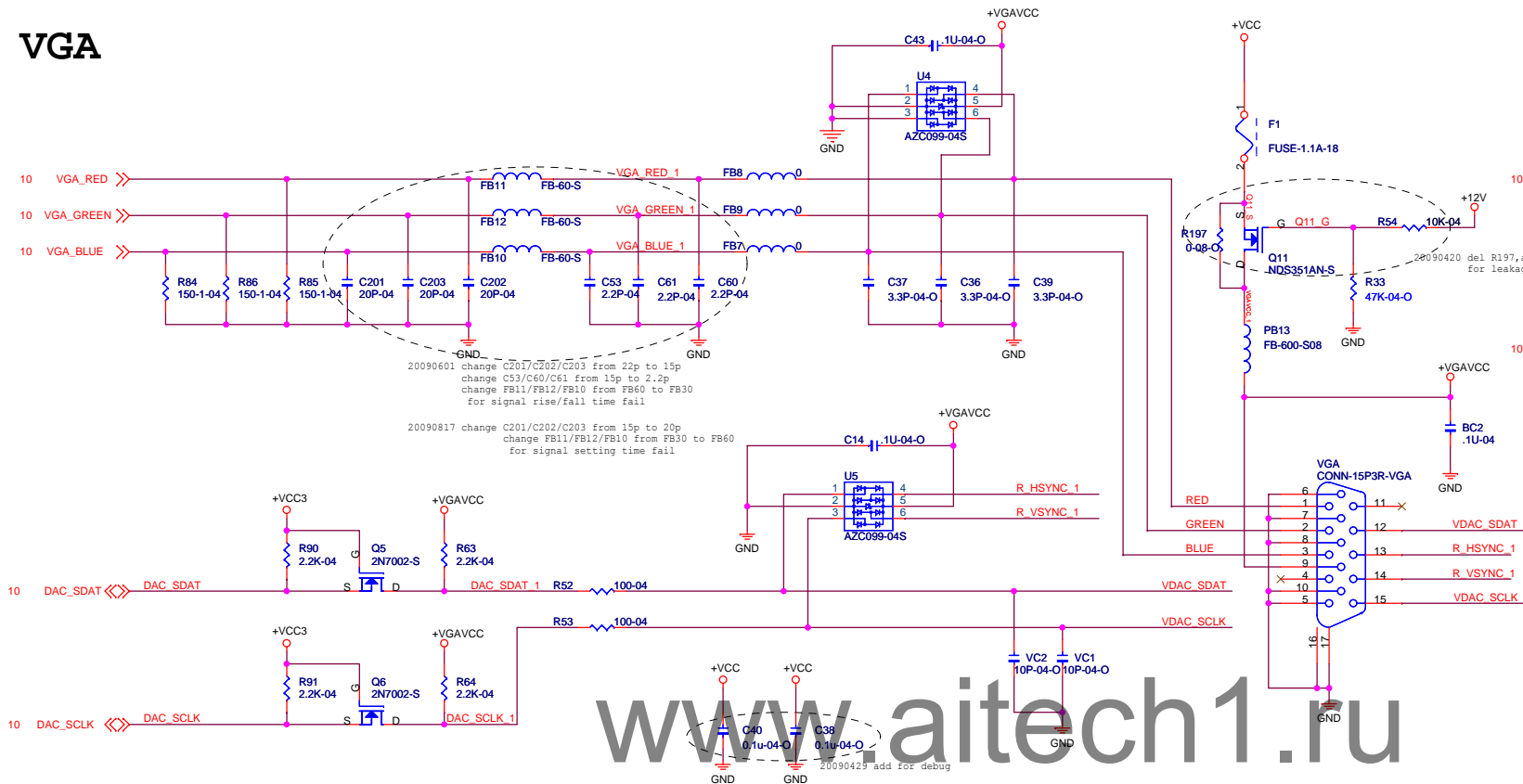


	OC_3	OC_2	OC_1	OC_0	Vswing (mV)	Pre/De-emphasis
*	0	0	0	0	500	0
	0	0	0	1	600	0
	0	0	1	0	750	0
	.	.	.	.		

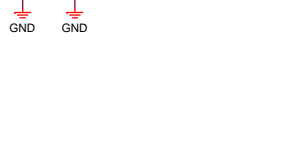
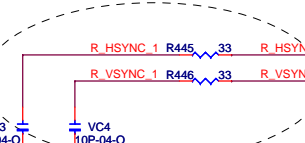
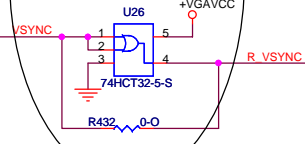
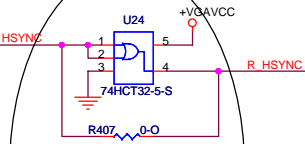




# VGA



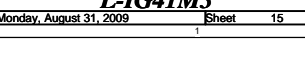
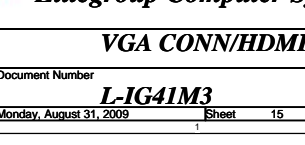
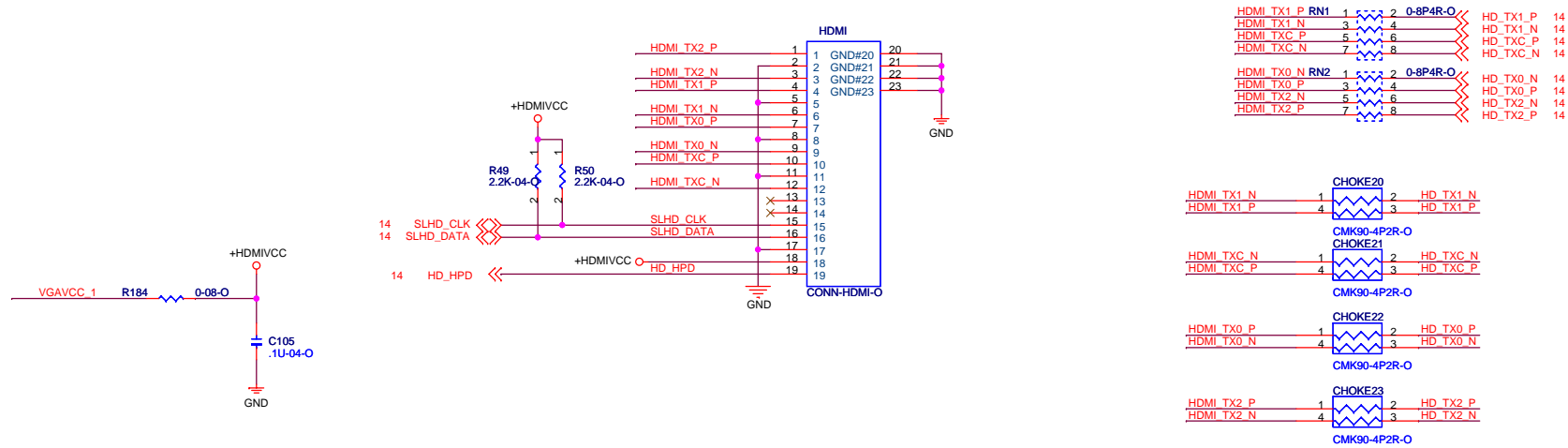
74HCT32-5-S  
02-192-032130 Better rise time  
02-192-032031 Better rise time



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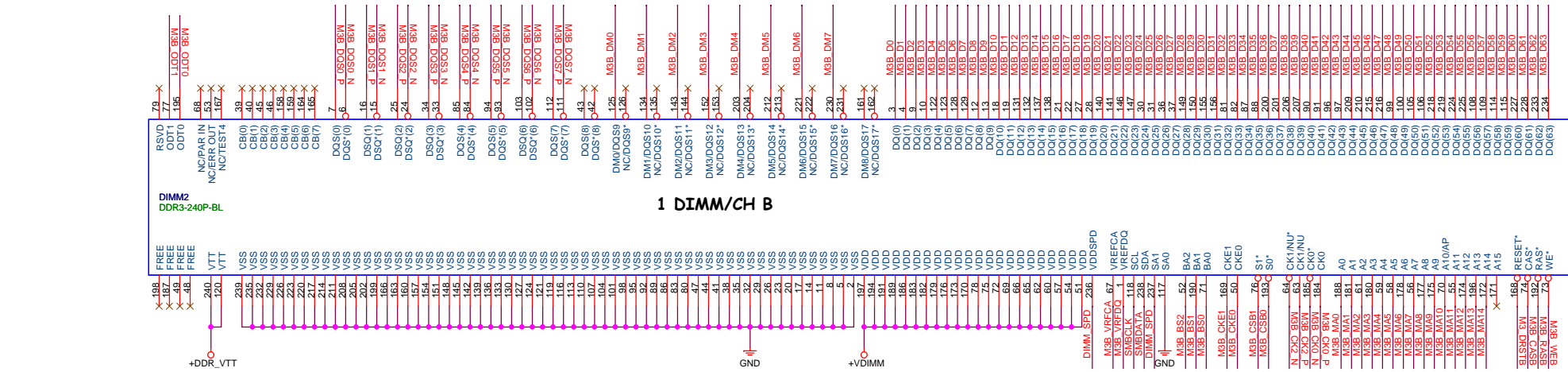
# HDMI

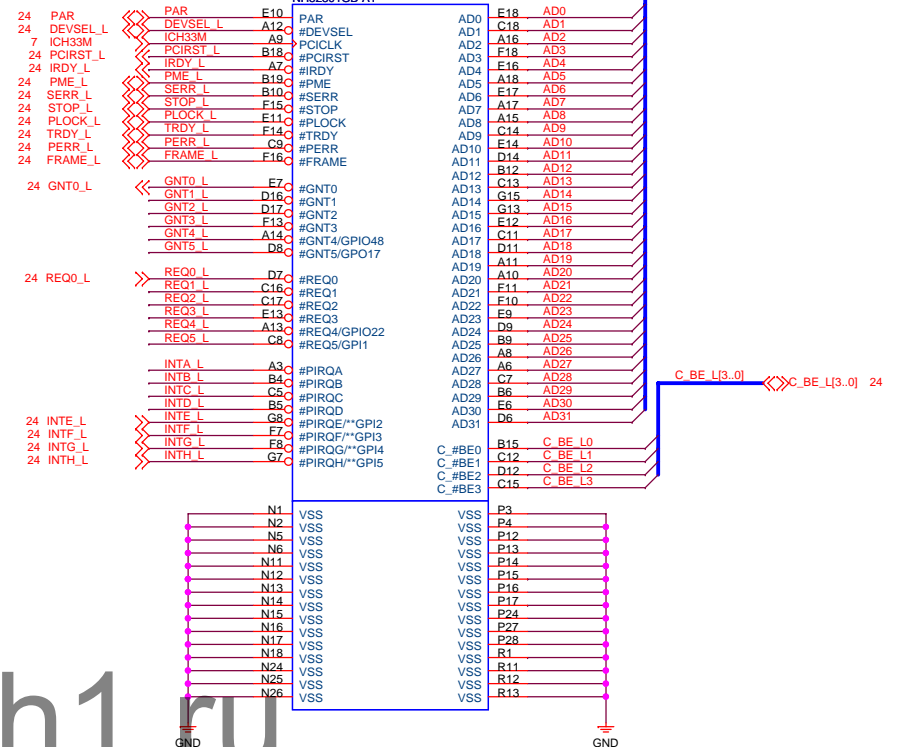
20090313 ADD





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Date: Monday, August 31, 2009 Sheet 18 of 38

The ICH7 3 GB/s SATA transmit buffers have been designed to maximize performance. As a result, the SATA transmit signaling voltage levels may exceed the TX and RX voltage specifications.  
(Reference Intel ICH7 Family Specification Update, Document Number: 307014-024, Page 13.)

7 SATA100M\_P  
7 SATA100M\_N

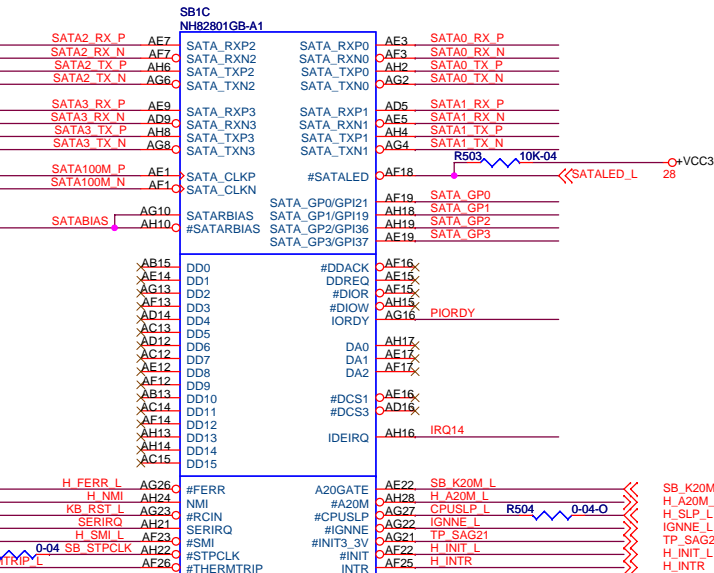
R493 24.9-1-04

SATABIAS LENGTH NO LONGER THAN 200MIL TO RESISTOR

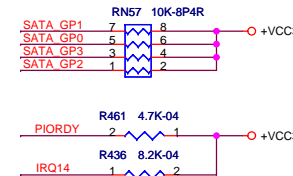
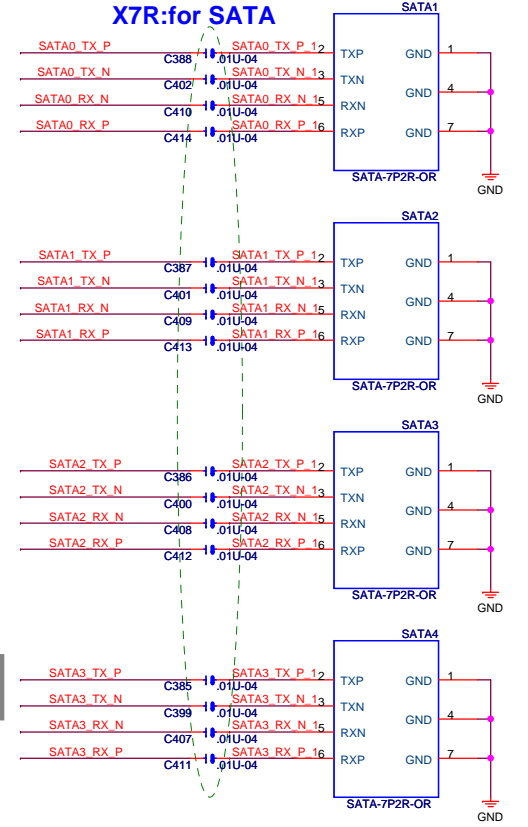
+FSB\_VTT

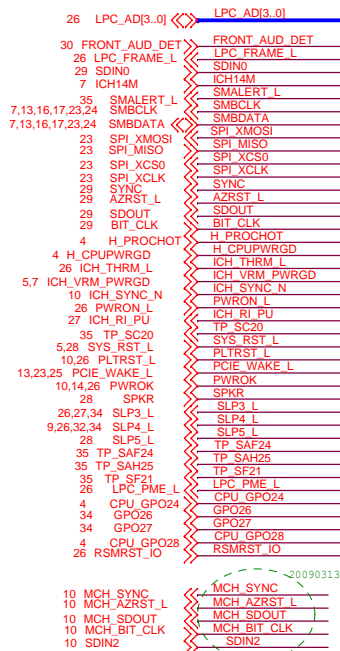
R487 62-04 H\_THERMTrip\_L  
R481 62-04 H\_FERR\_L

Place at ICH END of Route

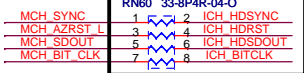


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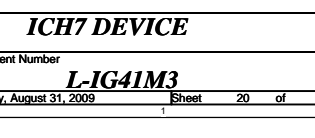
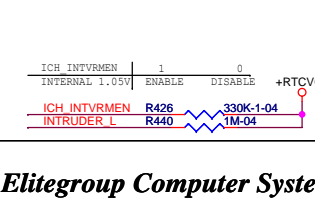
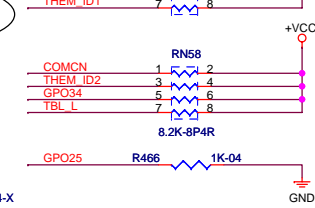
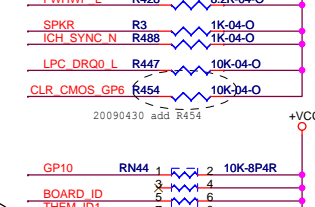
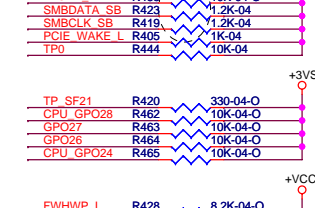
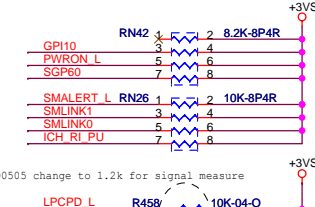
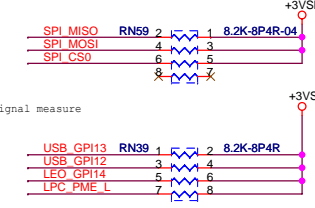
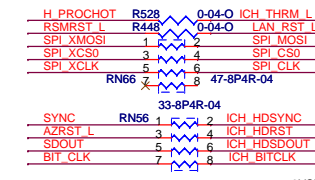
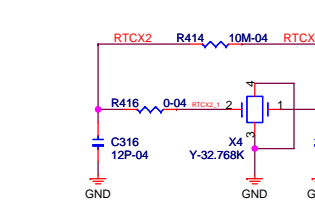
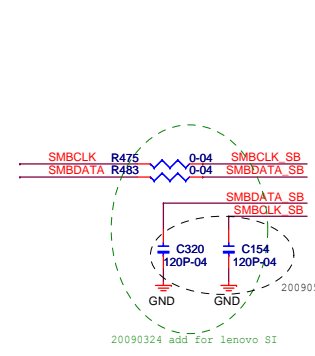
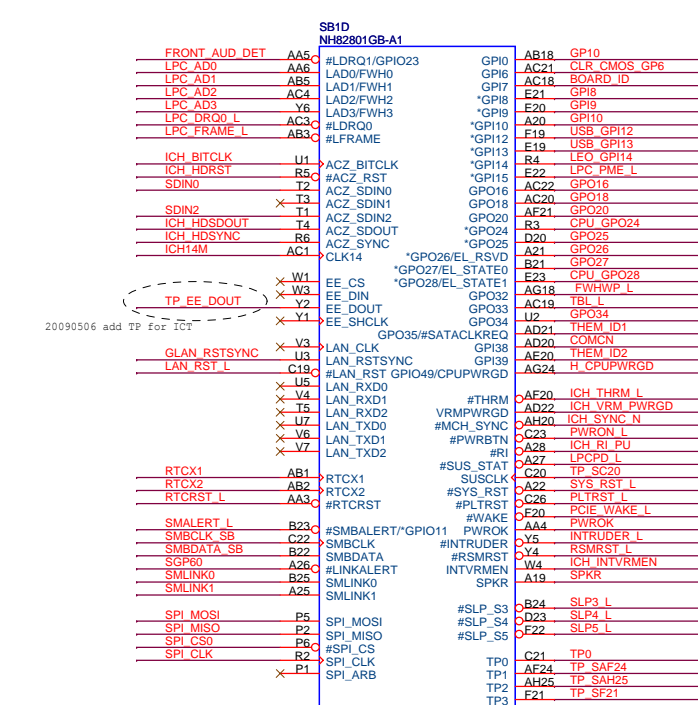




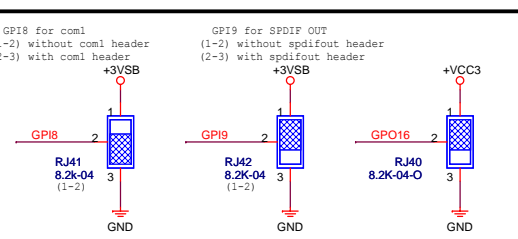
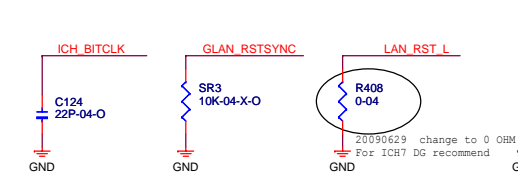
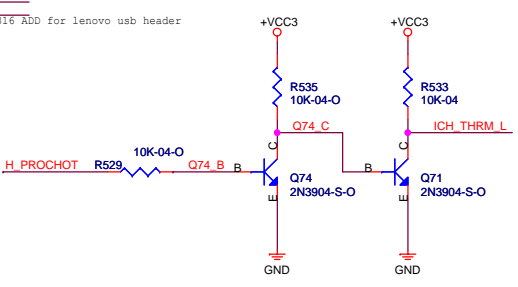
HDMIe



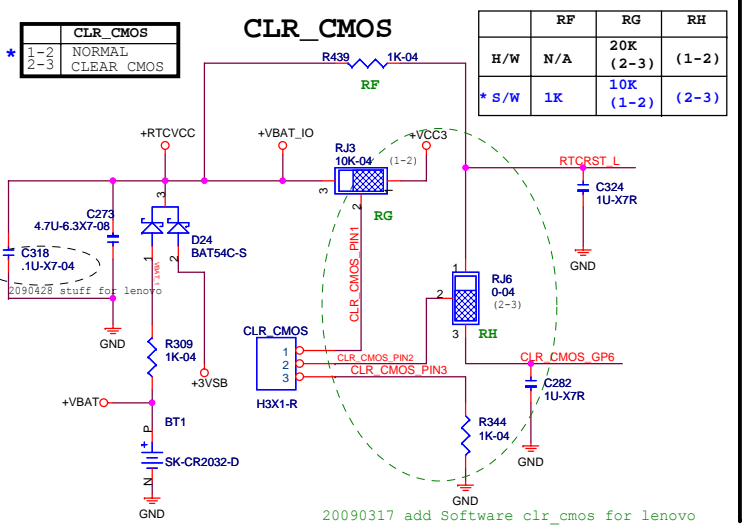
10 TP\_EE\_DOUT <<> TP\_EE\_DOUT



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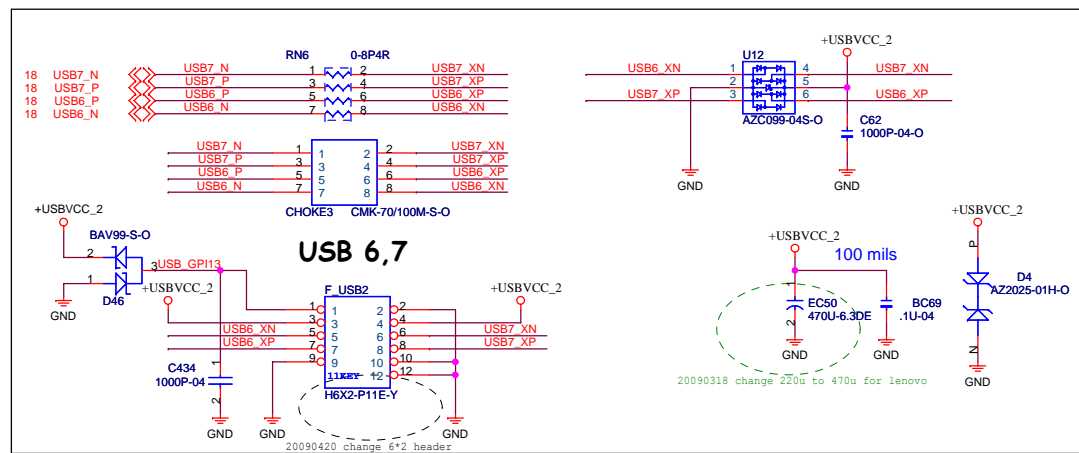
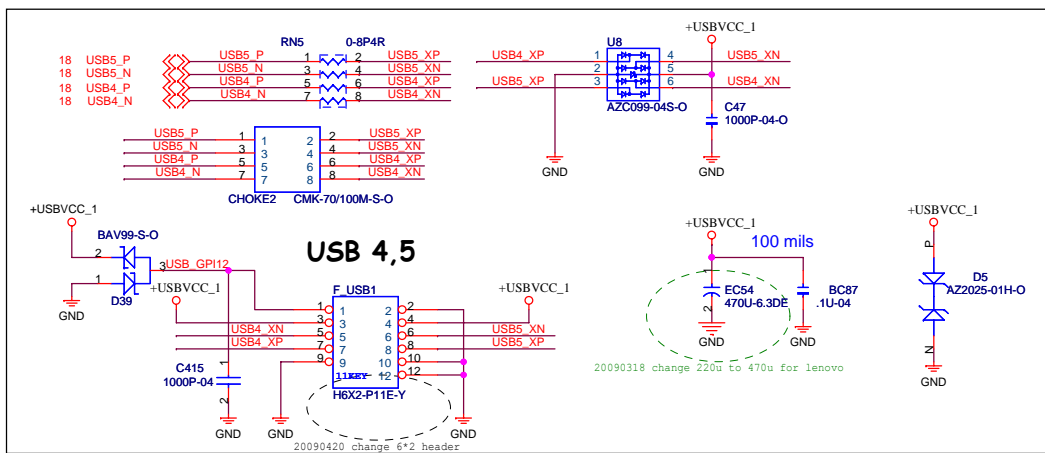


Reserve GPIO





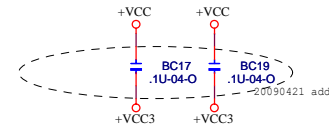
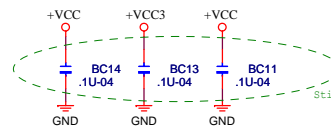
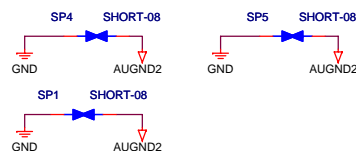
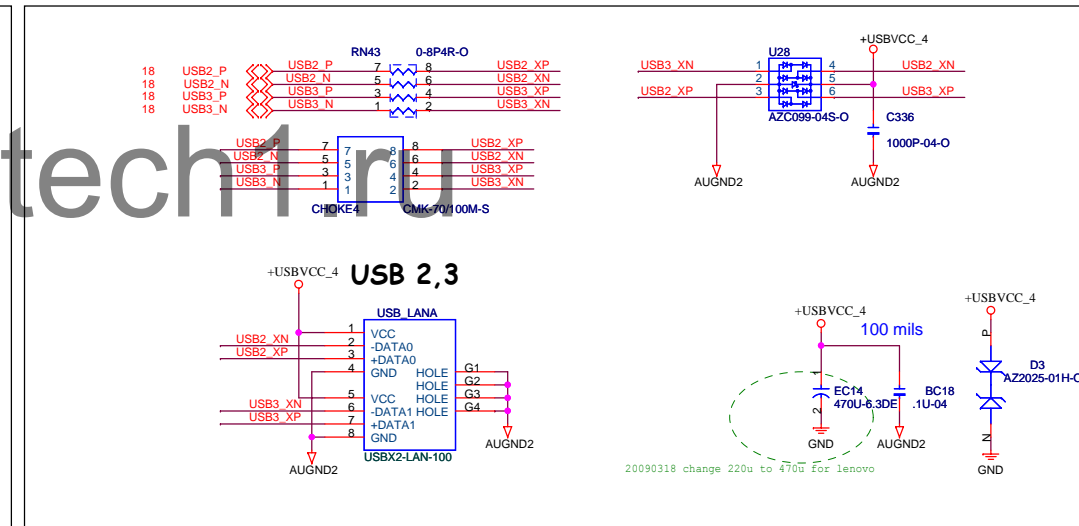
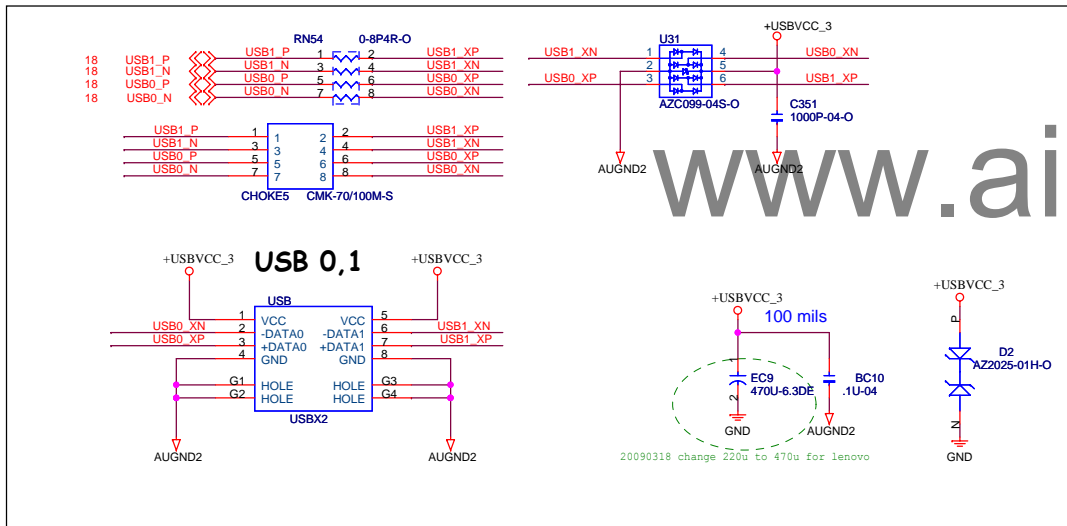


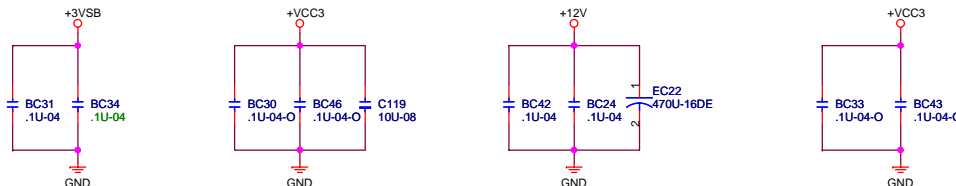
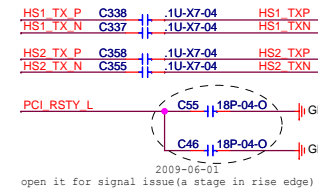
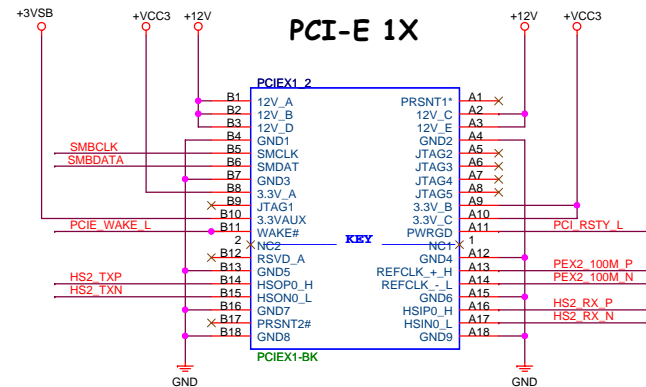
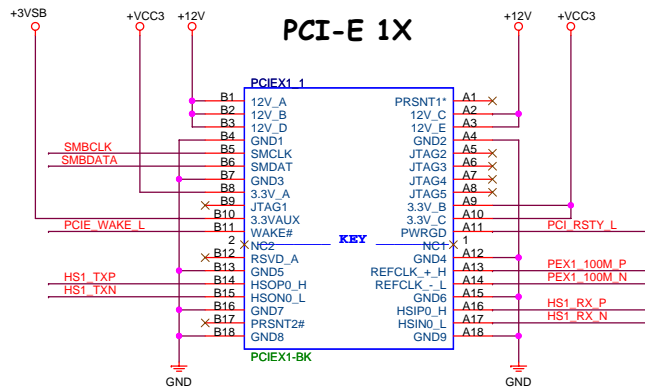
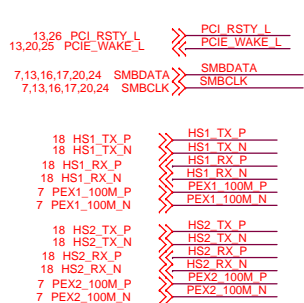


20 USB\_GPI13 USB\_GPI13  
20 USB\_GPI12 USB\_GPI12

20090316 Add for lenovo usb header

Lenovo request  
F\_USB1: UHCI HOST CONTROLLER 3#  
F\_USB2: UHCI HOST CONTROLLER 4#  
REAR\_USB: UHCI HOST CONTROLLER 1# ~ 2#



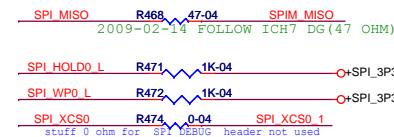
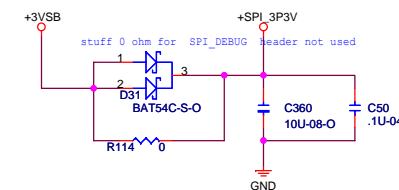


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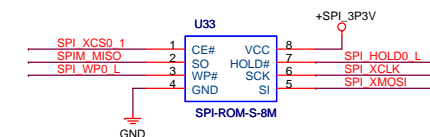
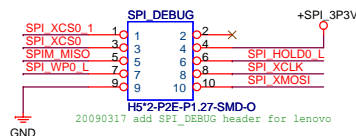


**SPI ROM**

2009-03-20 DEL TCM



**STUFF SPI\_DEBUG:**  
**DEL R474**  
**ADD D31,DEL R114(REWORK )**  
**ADD SPI\_DEBUG(1-3)**

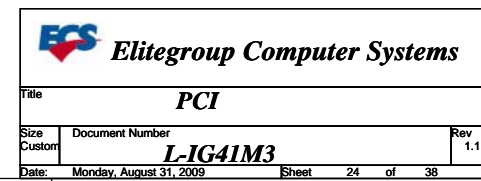


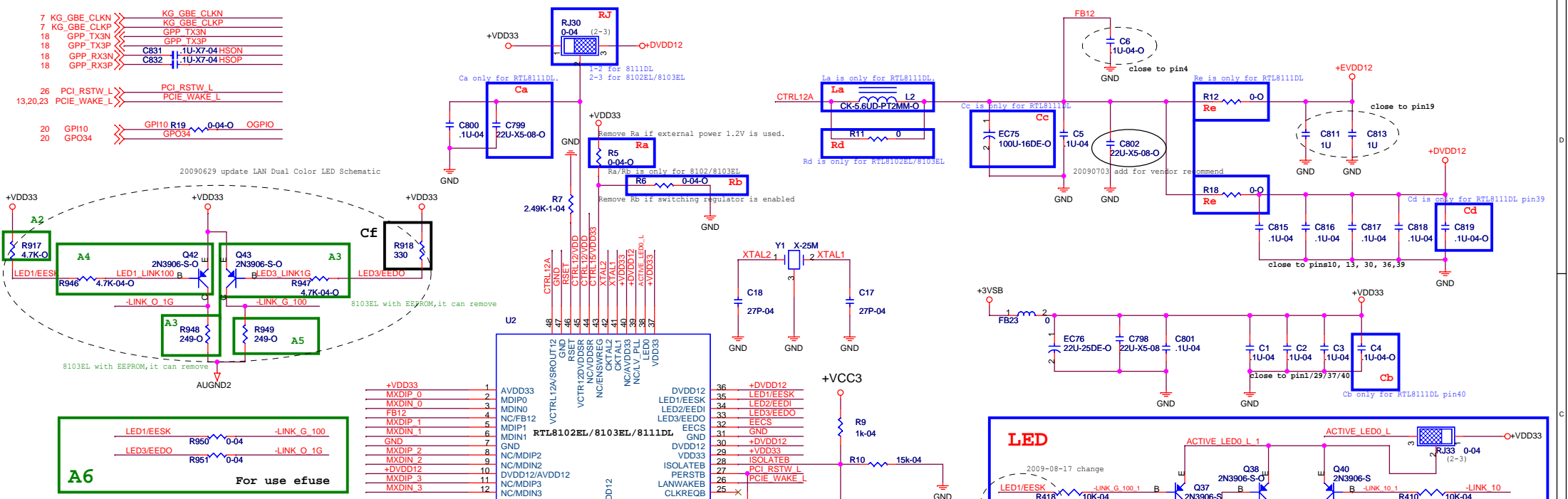
**Elitegroup Computer Systems**

Title **SPI ROM/PCI-E 1X \* 2**

Size Custom Document Number **L-IG41M3** Rev 1.1

Date Monday, August 31, 2009 Sheet 23 of 38





BOM Difference

Location	RTL8102EL RTL8103EL	RTL8111DL 1000M
Ra	X	V
Rb	X	X
Rc	V	X
Rd	V	X
La	X	V
Re	X	V
Ca	X	V
Cb	X	V
Cc	X	V
Cd	X	V
Ce	USBX2-LAN-100	USBX2-LAN-1000
Cf	V	X
Cg	.01U-04	0-04
RJ	(2-3)	(1-2)
LED	Not change	ADD R402/Q38
LAN IC	8102/8103EL	RTL8111DL

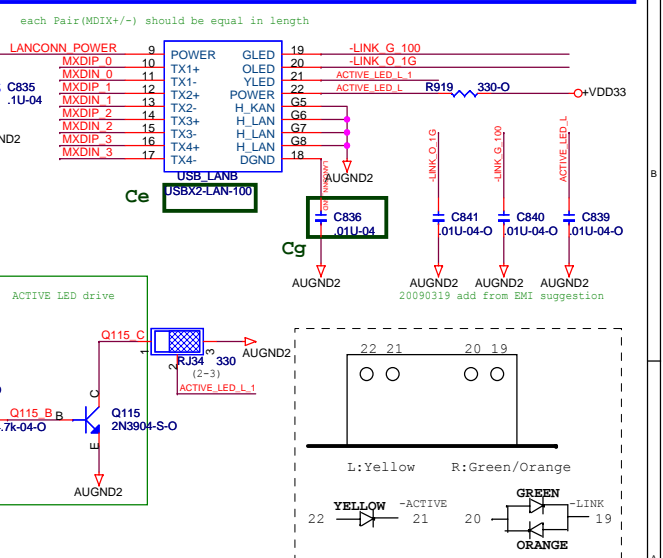
Location	USE EFUSE	USE EEPROM
Cf	330 OHM	4.7K OHM only stuff for 8111DL
A1	X	V
A2	X	V
A3	X	only stuff for 8111DL
A4	X	V
A5	X	V
A6	V	X

Location	RTL8111DL	RTL8102EL RTL8103EL
VDD33	3.3V	3.3V
AVDD12	1.05V	N/A
EVDD12	1.05V	1.2V
DVDD12	1.05V	1.2V

LEDs I/O	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	LINK10/ACT
LED1	LINK100	LINK100/1000	LINK	LINK100/ACT
LED2	LINK10	LINK10/100	Rx	FULL
LED3	LINK1000	LINK1000	FULL	LINK1000/ACT

LEDs I/O	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	Tx
LED1	LINK100	LINK	LINK	LINK100
LED2	LINK10	FULL	Rx	LINK10
LED3	NA	NA	NA	NA

WOL	Status	Yellow	Grn/Org
don't care	No Link	off	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off	off
on	10M,inactive	off	off
on	10M,active	off	off
on	100M,inactive	off	off
on	100M,active	off	off
on	1G,inactive	off	off
on	1G,active	off	off



**Elitegroup Computer Systems**

File: **REALTEK LAN 8102EL/8103EL/8111DL**

Size: Custom Document Number: **L-IG41M3** Rev: 1.1

Date: Monday, August 31, 2009 Sheet: 25 of 38

27 RTS-A <>> RTS-A  
27 DSR-A <>> DSR-A  
27 SOUTA <>> SOUTA  
27 SINA <>> SINA  
27 DTR-A <>> DTR-A  
27 DCD-A <>> DCD-A  
27 RIA <>> RIA  
27 CTS-A <>> CTS-A

28 FAN\_TAC1 <>> FAN\_TAC1  
28 FAN\_PWM1 <>> FAN\_PWM1  
28 FAN\_TAC2 <>> FAN\_TAC2  
28 FAN\_PWM2 <>> FAN\_PWM2

4 H\_THERMDA <>> H\_THERMDA  
4 H\_THERMDC <>> H\_THERMDC

27 MCLK <>> MCLK  
27 MDATA <>> MDATA  
27 KCLK <>> KCLK  
27 KDATA <>> KDATA

28,34 ATX\_PWRGD <>> ATX\_PWRGD  
10,14,20 PWROK <>> PWROK

25 PCI\_RSTW\_L <>> PCI\_RSTW\_L  
13,23 PCI\_RSTY\_L <>> PCI\_RSTY\_L  
9,20,32,34 SLP4\_L <>> SLP4\_L  
28,33 ATX\_PSON\_L <>> ATX\_PSON\_L  
28 PWRSTN\_L <>> PWRSTN\_L  
20 LPC\_PME\_L <>> LPC\_PME\_L  
20 PWRON\_L <>> PWRON\_L  
19 SB\_K20M\_L <>> SB\_K20M\_L  
19 KB\_RST\_L <>> KB\_RST\_L  
10,20 PLTRST\_L <>> PLTRST\_L  
19 SERIRQ <>> SERIRQ  
20 LPC\_FRAME\_L <>> LPC\_FRAME\_L  
20,27,34 SLP3\_L <>> SLP3\_L  
4 H\_PECI <>> H\_PECI

20 LPC\_AD[3..0] <>> LPC\_AD[3..0]

34 GPIO\_S4\_S5 <>> GPIO\_S4\_S5  
28 WT\_BEEP <>> WT\_BEEP  
20 ICH\_THRM\_L <>> ICH\_THRM\_L  
28 A\_GP26 <>> A\_GP26  
28 A\_GP25 <>> A\_GP25

7 SIO33M <>> SIO33M  
7 SIO48M <>> SIO48M

20 RSMRST\_IO <>> RSMRST\_IO

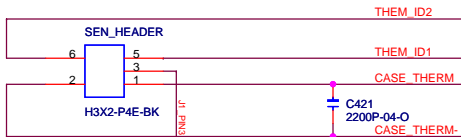
The RSMRST# signal of the Intel® ICH7 must transition from 20V signal level to 80V signal level and vice versa in 50 µs or less, and the falling edge must transition to 0.8 V or less before VccSus3\_3 drops to 2.1V

20 THEM\_ID2 <>> THEM\_ID2  
20 THEM\_ID1 <>> THEM\_ID1

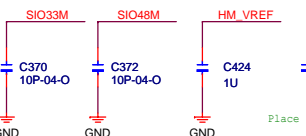
PWROK\_IO 0-04 R478 PWROK

C417 .1U-04-O

GND

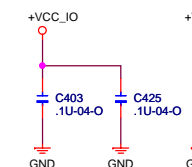


THEM_ID1	THEM_ID2	Chassic type
0	0	10L
0	1	13L
1	0	17L
* 1	1	25L

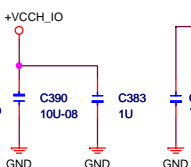


Place it close to 8755 pin49

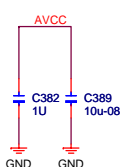
Close to pin31



Close to pin2,15



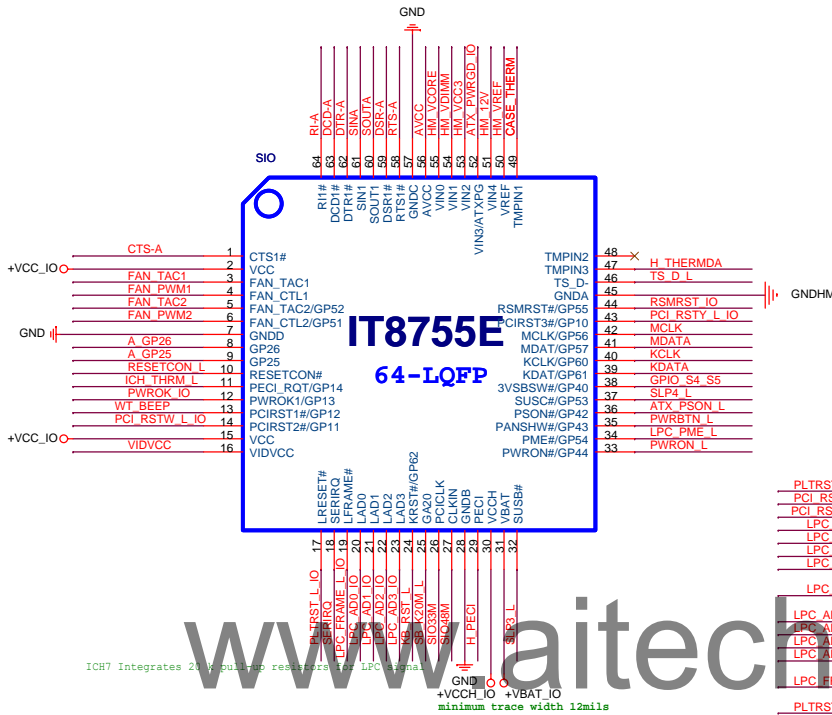
Close to pin30



Close to pin56

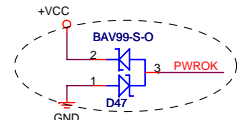
If without use these pins, Please pull-up to VCC. Don't let it floating

- 1.Pin 52:VIN3/ATXP3G
- 2.Pin 32:SUSB#
- 3.Pin 25/ Pin 58/ Pin 60/ Pin 62
- 4.Pin 10:RESETCON#



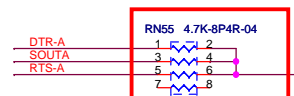
ICH7 Integrates 20V pullup resistors for LPC signal

+VCC3\_IO +VBAT\_IO minimum trace width 12mils



20090421 LENOVO SUGGESTION

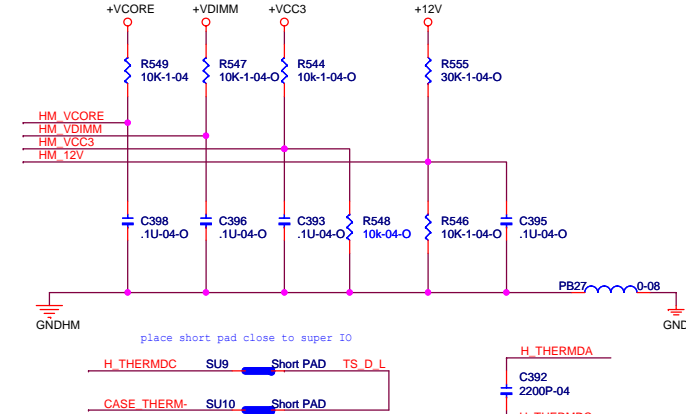
RN55 Stuff when COM1 not stuff



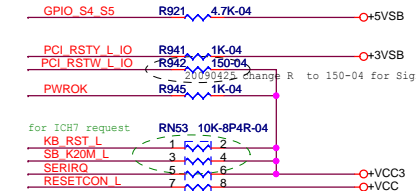
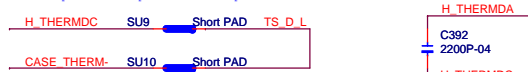
AVCC PB25 FB120-06 +AVCC\_IO

# BOM Difference

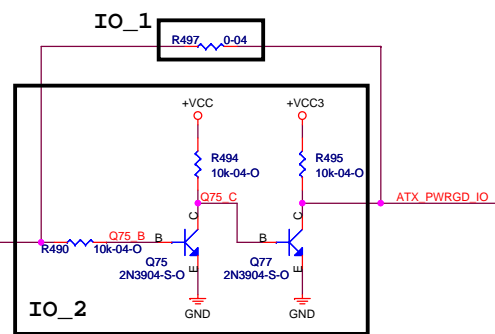
	IT8755	IT8757
IO_1	V	X
IO_2	X	V
IO_3	V	X
IO_4	X	V
IO_5	(2-3)	(1-2)



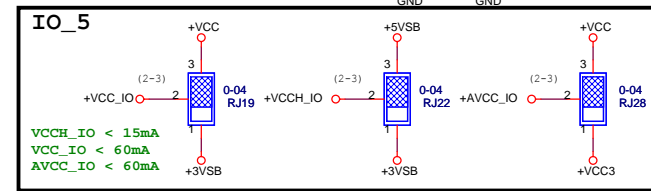
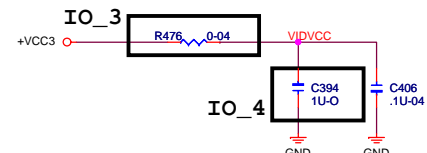
place short pad close to super IO



for ICH7 request  
KB\_RST\_L  
SB\_K20M\_L  
SERIRQ  
RESETCON\_L



20090629 Update IT8757 ATXP3G circuit for 3V level



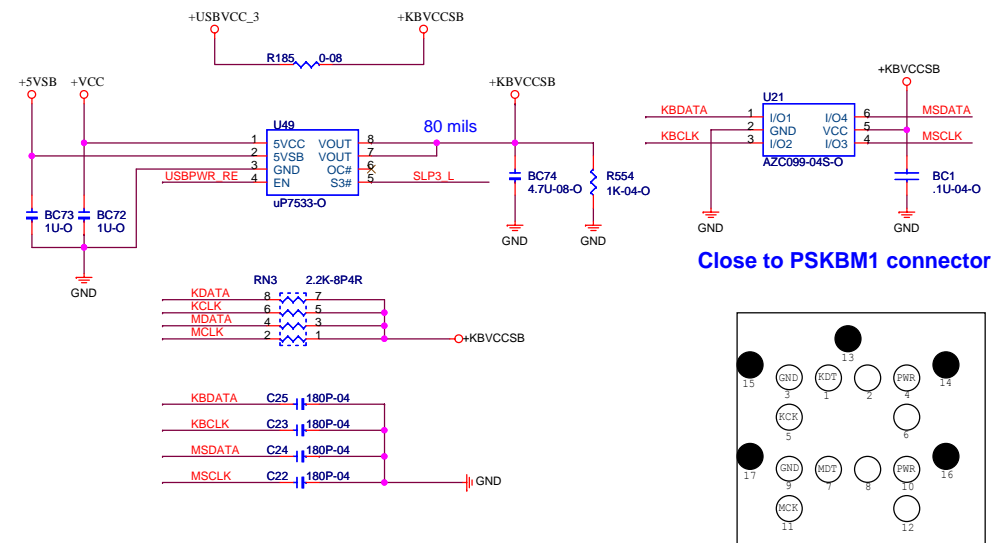
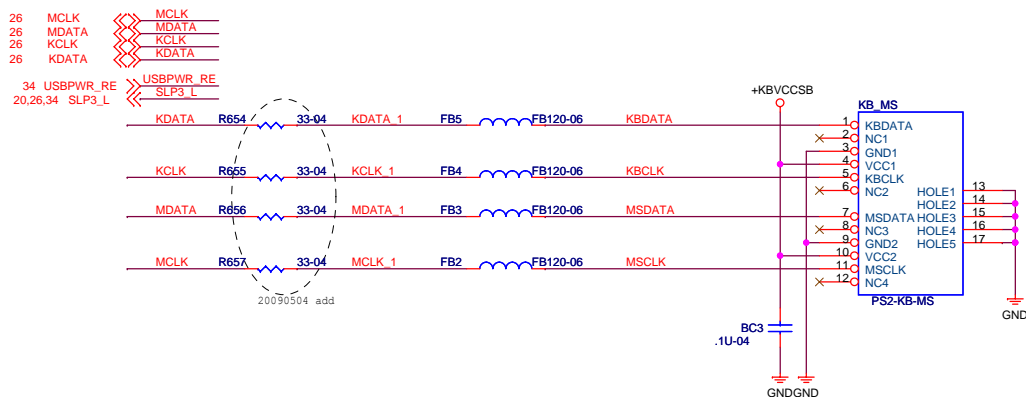
Model: SIO:IT8755/8757

Size: Custom Document Number: L-IG41M3

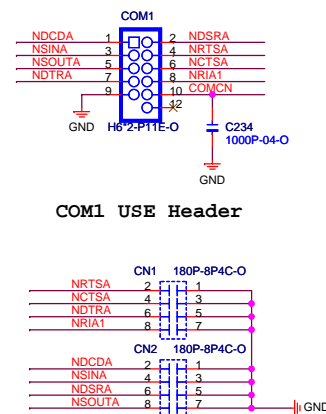
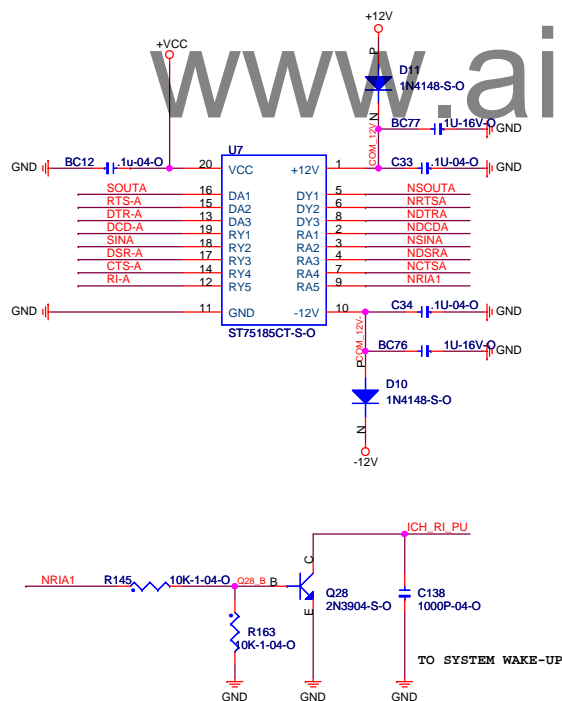
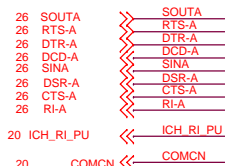
Date: Monday, August 31, 2009 Sheet: 26 of 38

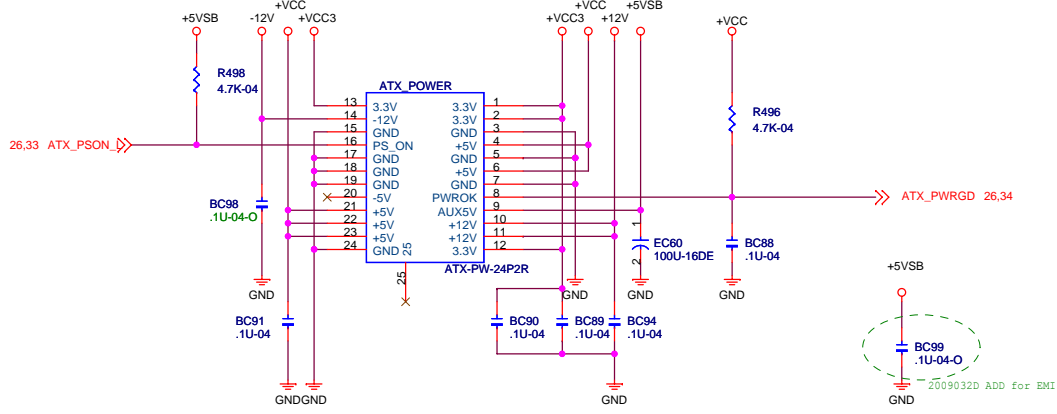


# KEYBOARD & MOUSE

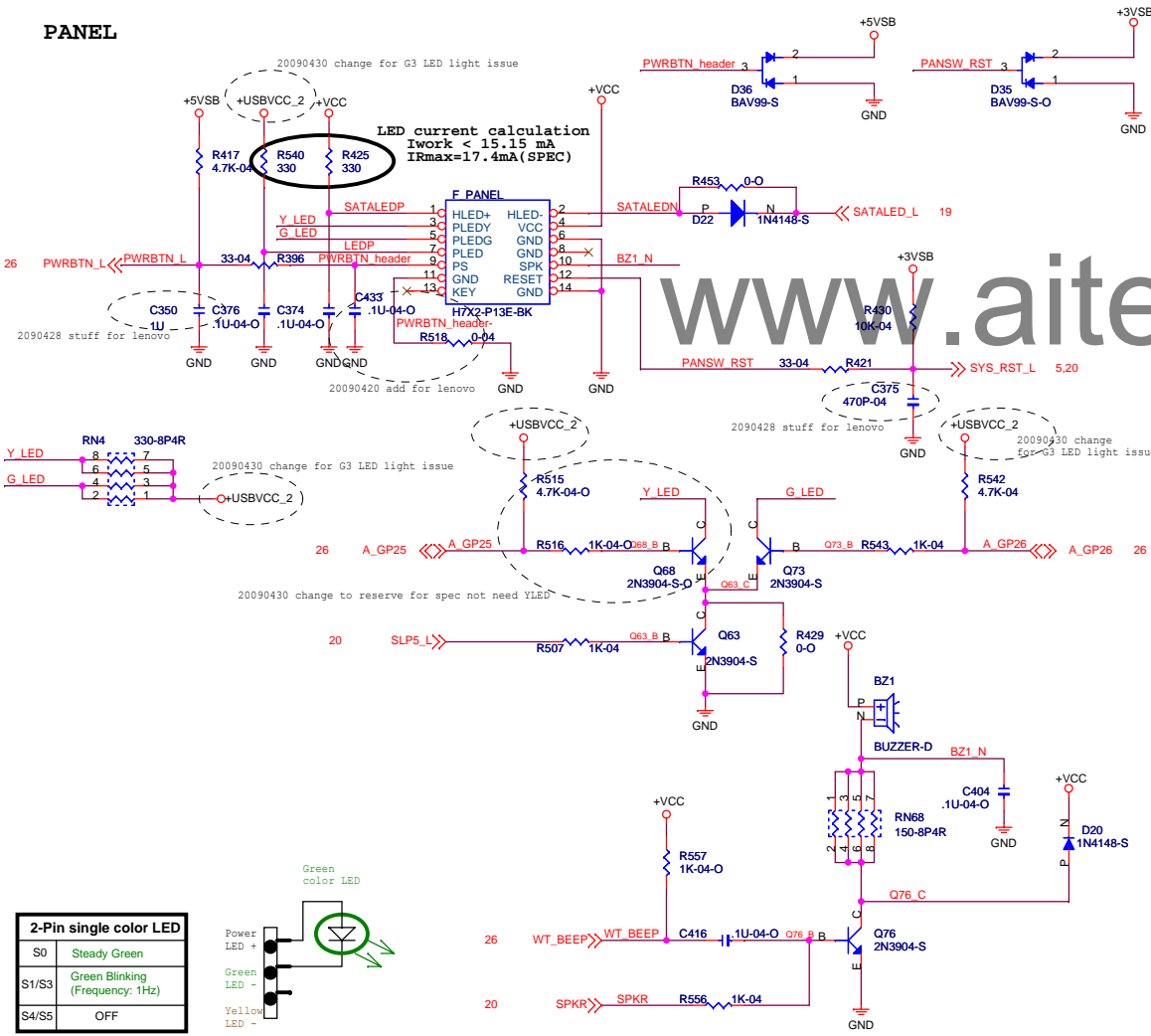


# COM1

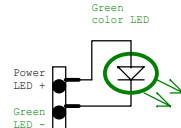




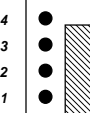
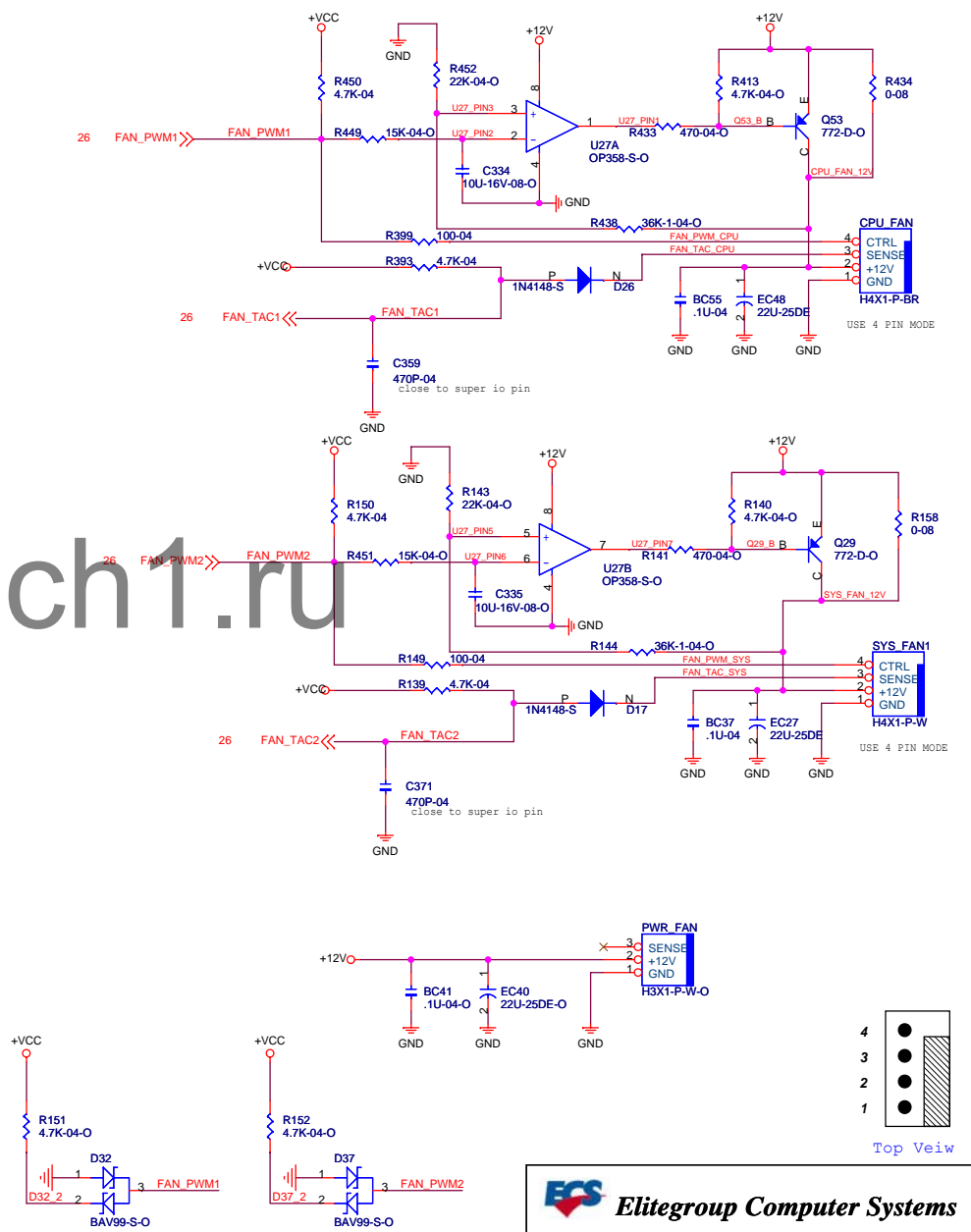
## PANEL



2-Pin single color LED	
S0	Steady Green
S1/S3	Green Blinking (Frequency: 1Hz)
S4/S5	OFF



## FAN



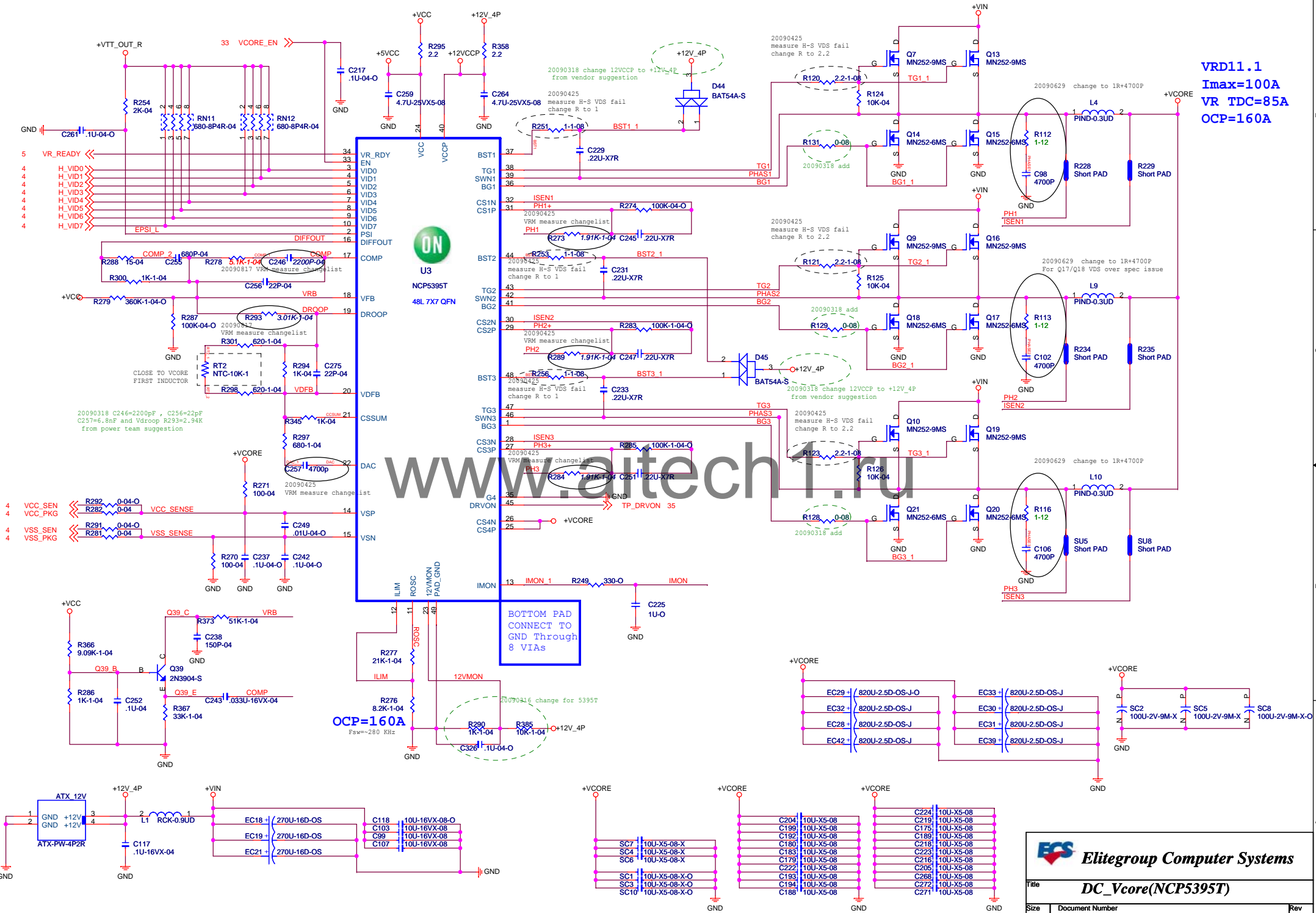
Top Veiv

**Elitegroup Computer Systems**

Title			<b>PANEL &amp; FAN</b>		
Size	Document Number				Rev
Custom	<b>L-IG41M3</b>			1.1	
Date:	Monday, August 31, 2009	Sheet	28	of	38








VRD11.1  
Imax=100A  
VR TDC=85A  
OCP=160A

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BOTTOM PAD  
CONNECT TO  
GND Through  
8 VIAs

OCP=160A  
Fsw=280 KHz

**Elitegroup Computer Systems**

Title

DC\_Vcore(NCP5395T)

Size

Document Number

Custom

L-IG41M3

Date

Monday, August 31, 2009

Sheet

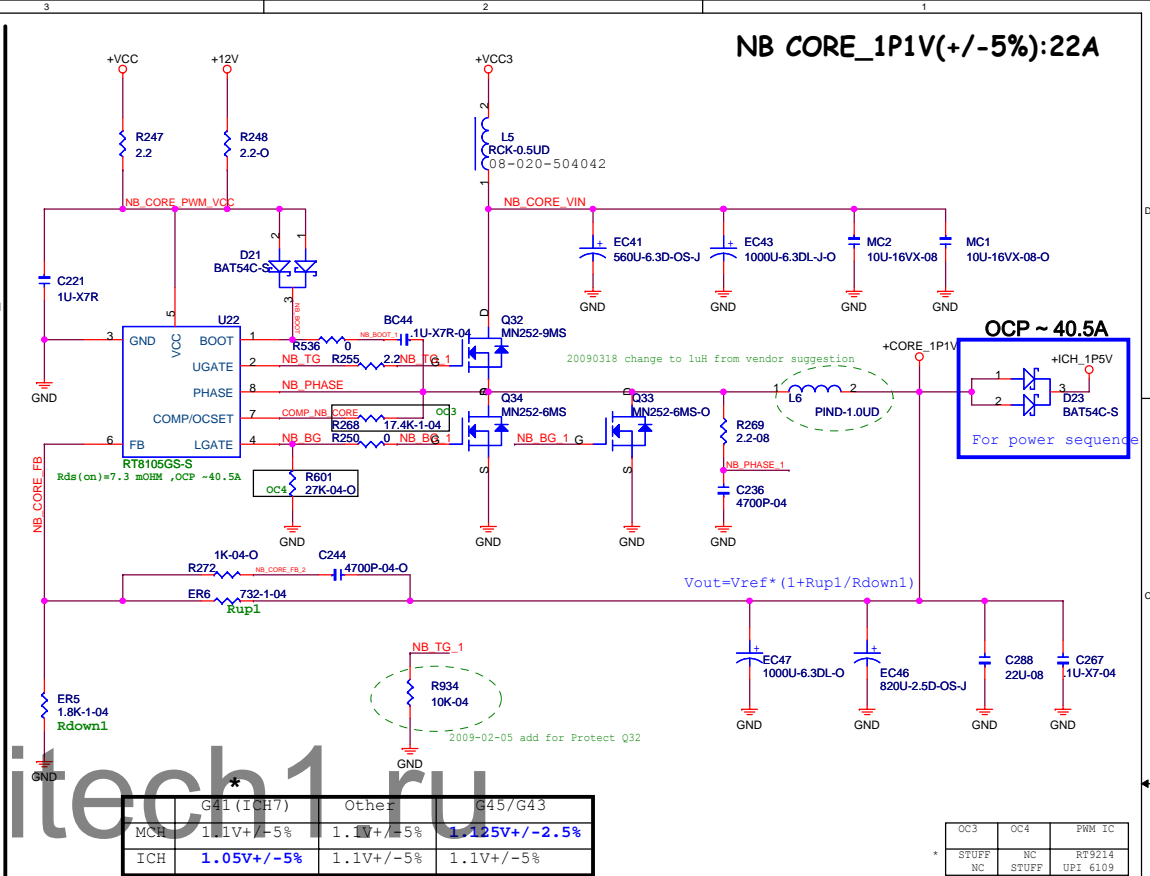
31

of

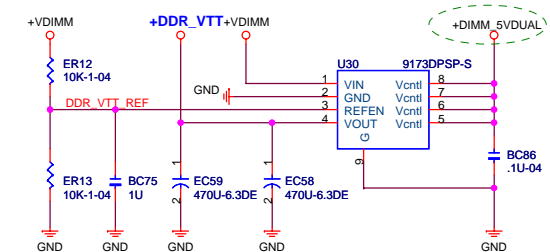
38

Rev

1.1



DDR\_VTT:1.2A







26 GPIO\_S4\_S5  
20 GPO26  
20 GPO27  
20,26,27 SLP3\_L  
9,20,26,32 SLP4\_L

26,28 ATX\_PWRGD  
27 USBPWR\_RE

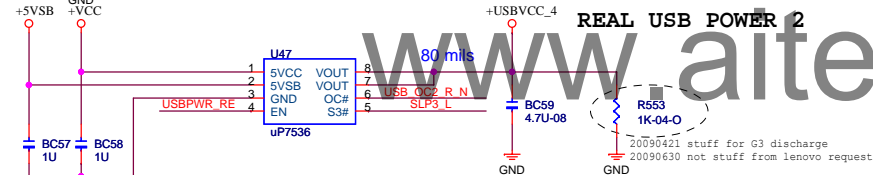
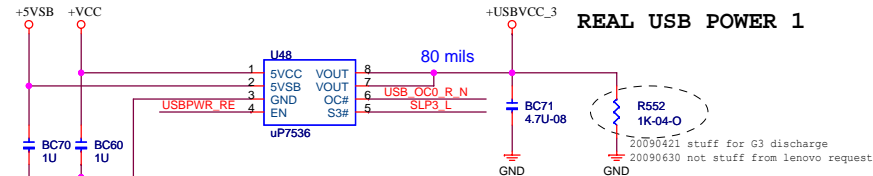
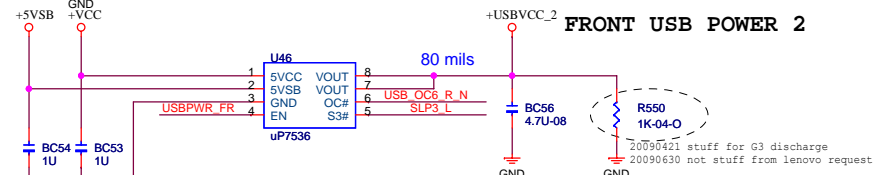
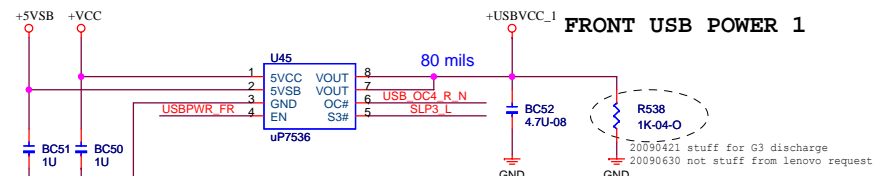
GPO26  
USBPWR\_FR  
SLP4\_L

GP26/GP27 is low when G3 to AC power plug

GPO27  
USBPWR\_RE  
SLP4\_L

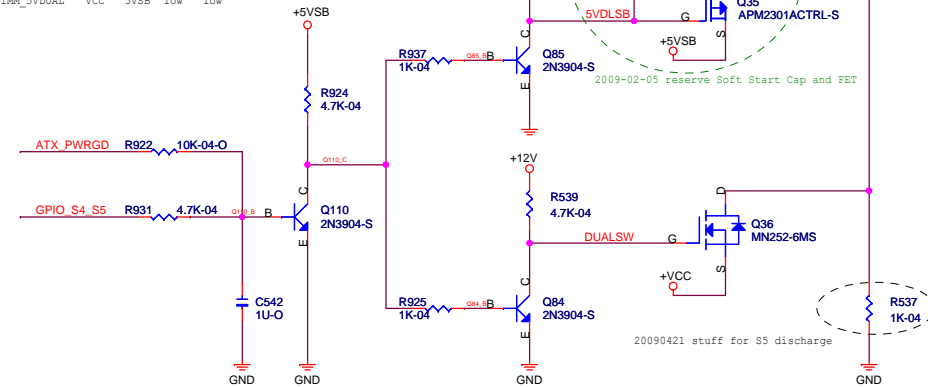
18 USB\_OC0\_R\_N  
18 USB\_OC2\_R\_N  
18 USB\_OC4\_R\_N  
18 USB\_OC6\_R\_N

20090324 add for lenovo

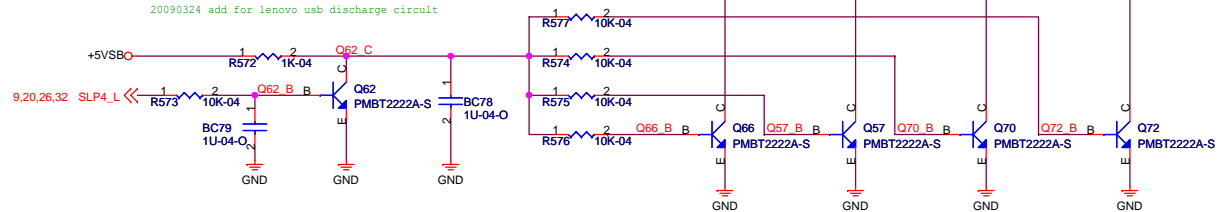


## DIMM\_5VDUAL

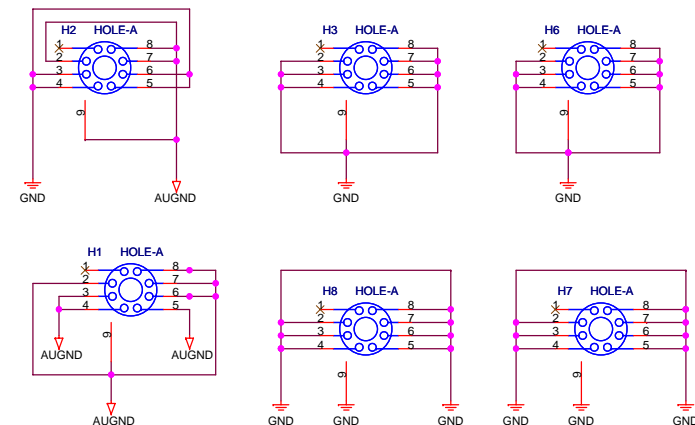
	S0	S3	S4	S5
GPIO_S4_S5	high	low	high	high
DIMM_5VDUAL	VCC	5VSB	low	low



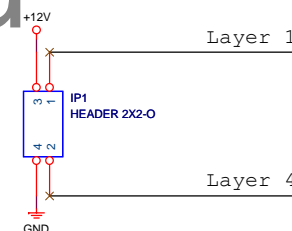
20090324 add for lenovo usb discharge circuit



remove the PSI# errata circuit (G41 not support C3/C4)

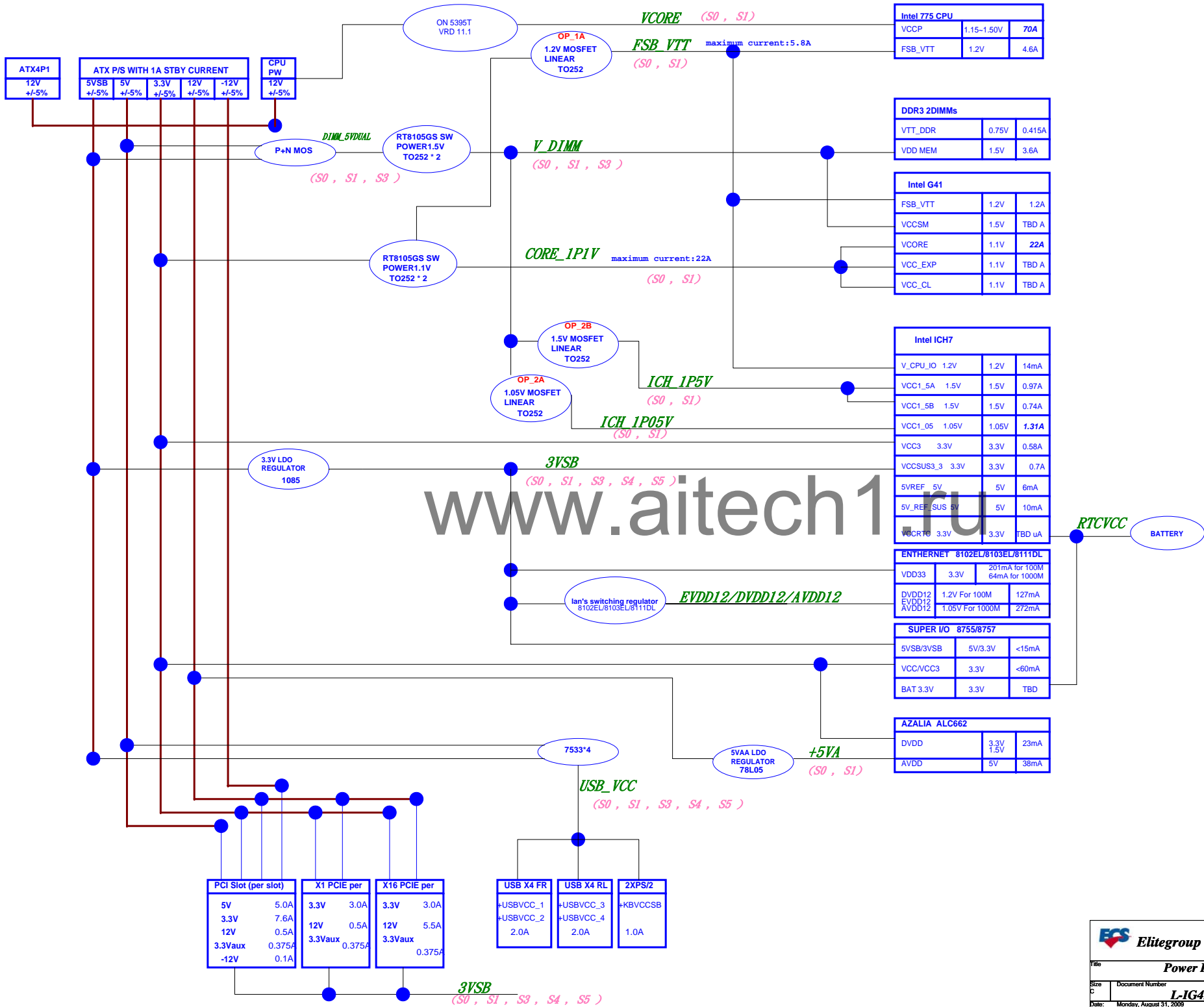


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**Elitegroup Computer Systems**

Date: Monday, August 31, 2009 Sheet 35 of 38



Intel 775 CPU		
VCCP	1.15~1.50V	70A
FSB_VTT	1.2V	4.6A

DDR3 2DIMMs		
VTT_DDR	0.75V	0.415A
VDD MEM	1.5V	3.6A

Intel G41		
FSB_VTT	1.2V	1.2A
VCCSM	1.5V	TBD A
VCORE	1.1V	22A
VCC_EXP	1.1V	TBD A
VCC_CL	1.1V	TBD A

Intel ICH7		
V_CPU_IO 1.2V	1.2V	14mA
VCC1_5A 1.5V	1.5V	0.97A
VCC1_5B 1.5V	1.5V	0.74A
VCC1_05 1.05V	1.05V	1.31A
VCC3 3.3V	3.3V	0.58A
VCCSUS3_3 3.3V	3.3V	0.7A
SVREF 5V	5V	6mA
SV_REF SUS 5V	5V	10mA
VCCRT6 3.3V	3.3V	TBD uA

ETHERNET 8102EL/8103EL/8111DL		
VDD33 3.3V	201mA for 100M 64mA for 1000M	
DVDD12 1.2V For 100M	127mA	
EVDD12 1.05V For 1000M	272mA	

SUPER I/O 8755/8757		
5VSB/3VSB 5V/3.3V	<15mA	
VCC/VCC3 3.3V	<60mA	
BAT 3.3V 3.3V	TBD	

AZALIA ALC662		
DVDD 3.3V 1.5V	23mA	
AVDD 5V	38mA	

BATTERY

